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TURBINE BLADE  
DATA ACQUISITION SYSTEM  
TECHNICAL REFERENCE

M. J. Gutman

University of Dayton Research Institute  
Electronic and Computer Development Laboratory  
300 College Park Avenue  
Dayton, OH 45469-0001

May 1989

Final Report for Period September 1985 to August 1987

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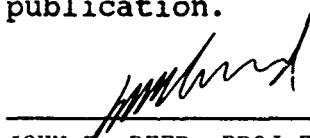
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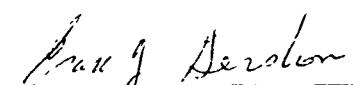
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\_\_\_\_\_  
JOHN D. REED, PROJ ENGR  
Assessment Branch  
Turbine Engine Division  
Aero Propulsion & Power  
Laboratory  
FOR THE COMMANDER

  
\_\_\_\_\_  
ISAK J. GERSHON, TAM  
Components Branch  
Turbine Engine Division  
Aero Propulsion & Power  
Laboratory

  
\_\_\_\_\_  
GEOFFREY W. JUMPER, Maj, USAF  
Chief, Components Branch  
Turbine Engine Division  
Aero Propulsion & Power  
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This report provides design and technical documentation on the Turbine Blade Data Acquisition System developed by the Electronic and Computer Development Laboratory, within the University of Dayton Research Institute. It was designed and fabricated as an analytical tool for structural testing and research on turbine components as part of the Noncontacting Stress Measurement System. This research effort was performed for the Aerospace Mechanics Group of the Research Institute. Michael Drake was the Principal Investigator and Robert Dominic was the Research Engineer in charge of daily activities for this project.

E&CD Lab personnel who contributed to this research and development effort were:

Lab Supervisor . . . . . G. Thomas Collins

Electronic Design . . . . . J. Michael Aulds  
Robert Blanchard

Fabrication and Checkout . . . . . Ben Connally  
Fred L. Davis  
Steve Fuchs

Documentation . . . . . Michael Gutman  
Steve Fuchs

Report Assembly . . . . . Sam Pietrantonio

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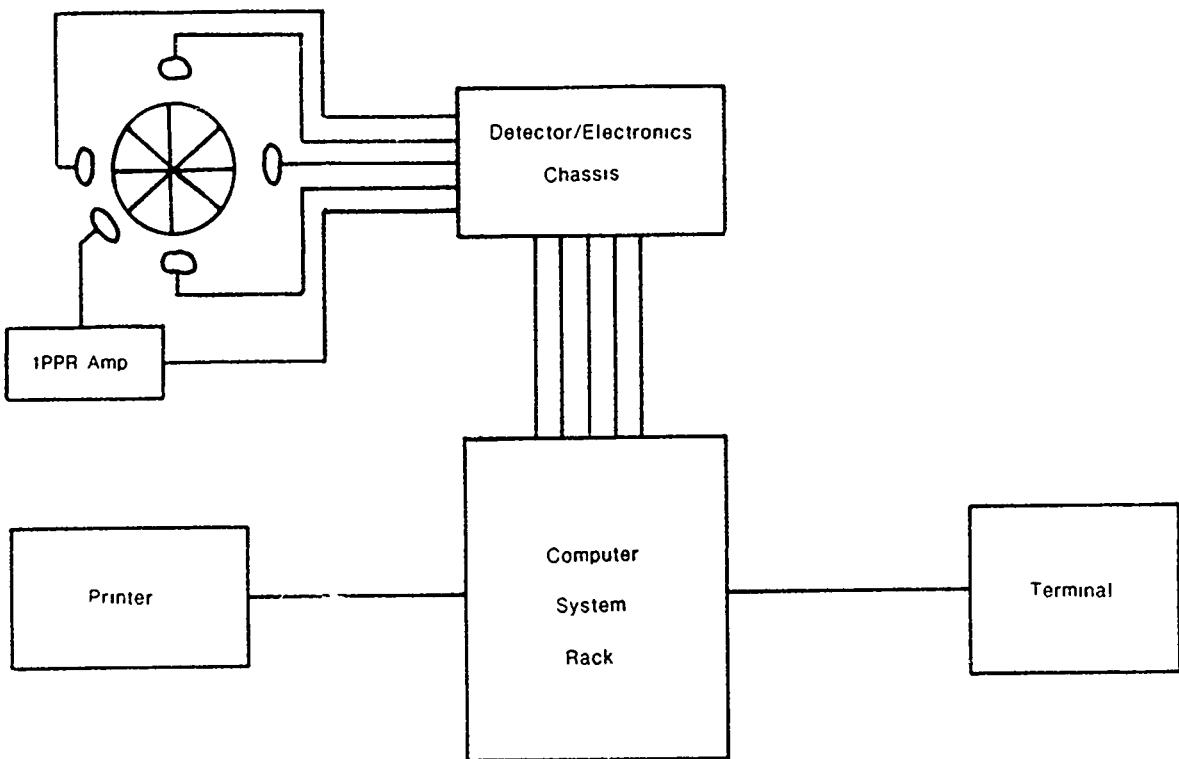


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TITLE TBDAS BLOCK DIAGRAM					FILENAME BLANK PLT	UDRI University of Dayton Research Institute Electronic & Computer Development Laboratory
FIGURE 1	SHEET 1 or 1	DESIGNER ECO	DRAWN BY MJG	FILEDATE 07-Jul-1989	FILETIME 07 49 06	
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Figure 1: TBDAS Block Diagram

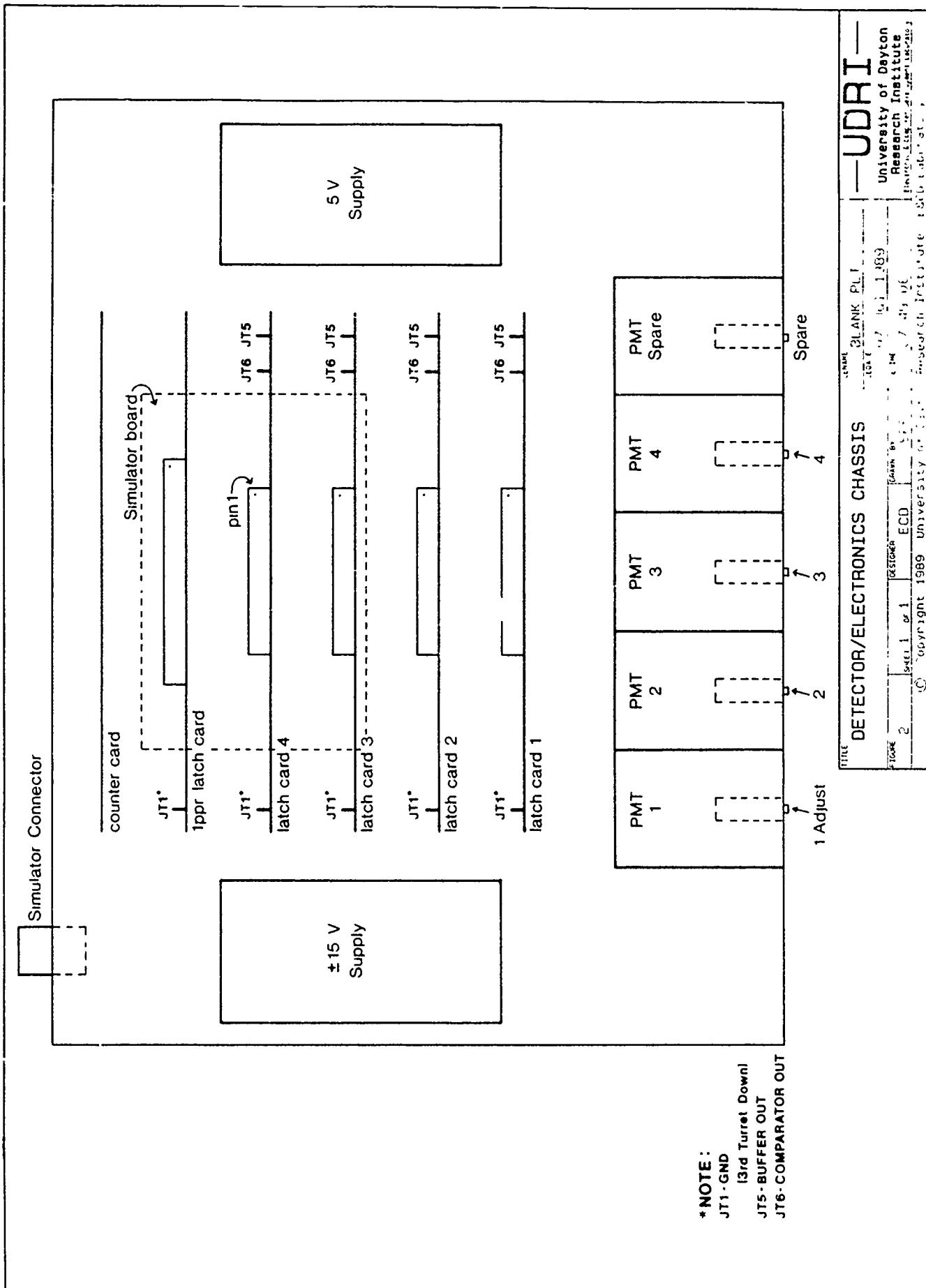


Figure 2: Detector/Electronics Chassis

# NSMS Data Acquisition System

C = Change Date / Time / Specimen Data

D = Discard Data

H = Histogram

P = Real Time Display

S = Start Taking Data

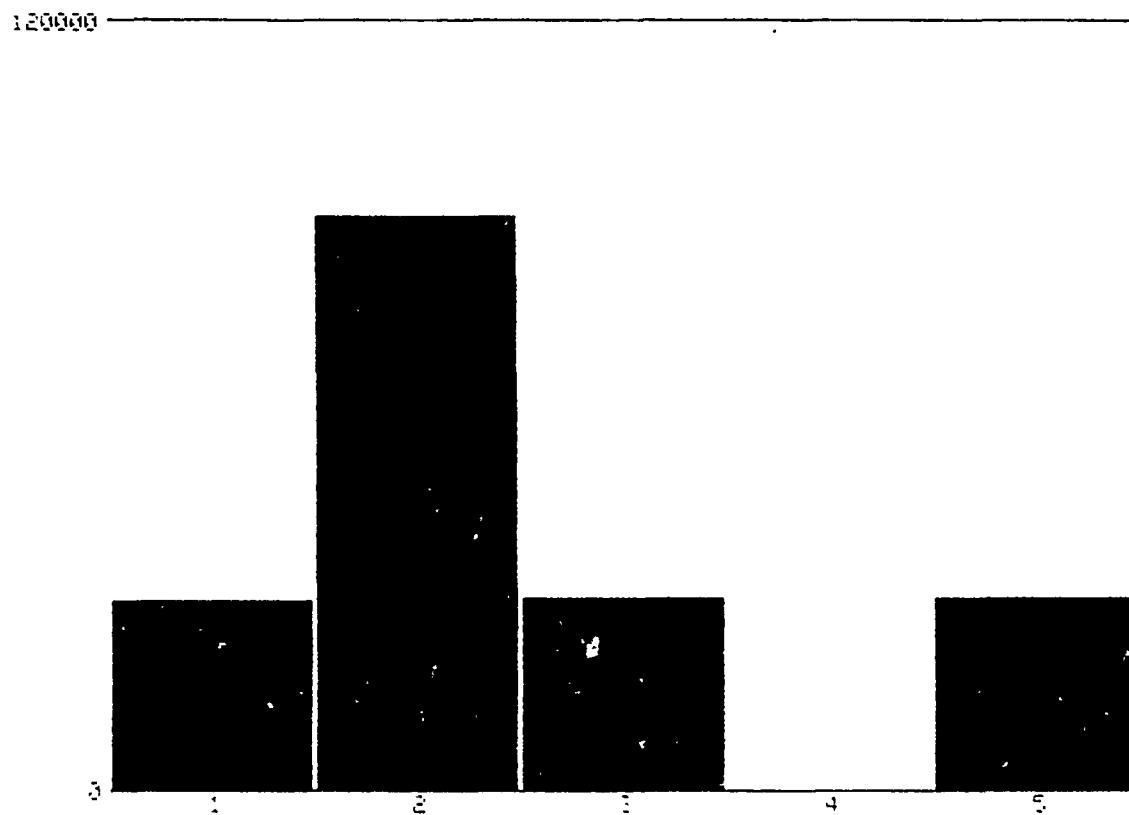
W = Write Data To Tape

TITLE <b>MAIN MENU TERMINAL DISPLAY</b>				FILENAME <b>BLANK PLT</b>	<b>UDRI</b> University of Dayton Research Institute Electronic & Computer Development Laboratory
FIGURE 3	HEET 1 of 1	DESIGNER	DRAWN BY	FILEDATE 07-Jul-1989	
				FILETIME 07 49 06	

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Figure 3: Main Menu Terminal Display

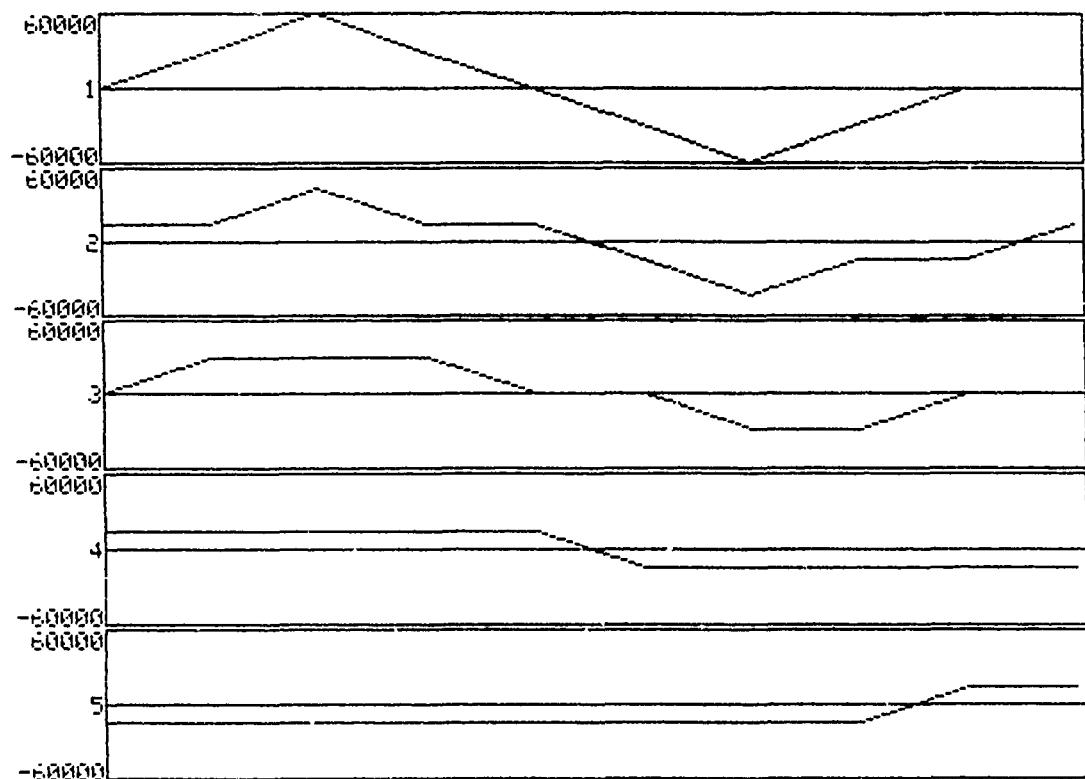
TEST RUN Station-1 625 Hz 625 RPM 13-Oct-87 08:54:40



TITLE HISTOGRAM TERMINAL DISPLAY				FILENAME BLANK.PLT	UDRI University of Dayton Research Institute Electronic & Computer Development Laboratory
FIGURE 4	1	DESIGNER	DRAWN BY	FILEDATE 07-Jul-1989	
	SHEET 1 OF 1			FILETIME 07 49 06	
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Figure 4: Histogram Terminal Display

TEST RUN Station-1 625 Hz 625 RPM 13-Oct-87 08:36:56



TITLE REAL TIME TERMINAL DISPLAY				FILENAME BLANK PLT	UDRI University of Dayton Research Institute Electronic & Computer Development Laboratory
FIGURE 5	Sheet 1 of 1	DESIGNER	DRAWN BY	FILEDATE 07-Jul-1989 FILETIME 07 49 06	
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Figure 5: Real Time Terminal Display

# NSMS Data Acquisition System

Resolution 204 of 1000

	Current	Minimum	Maximum
-----	-----	-----	-----
Speed :	625	625	625 RPM

C = Change Date Time < Specimen Data

D = Discard Data

H = Histogram

P = Real Time Display

S = Start Taking Data

W = Write Data To Tape

MAIN MENU RUN TIME TERMINAL DISPLAY				FILENAME	BLANK.PLT	
FIGURE	6	Sheet 1 of 1	DESIGNER	CREATED BY	DATE	17-JUL-1989
FIGURE	6	Sheet 1 of 1	DESIGNER	CREATED BY	FILETYPE	07-49-06
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Figure 6: Main Menu Run Time Terminal Display

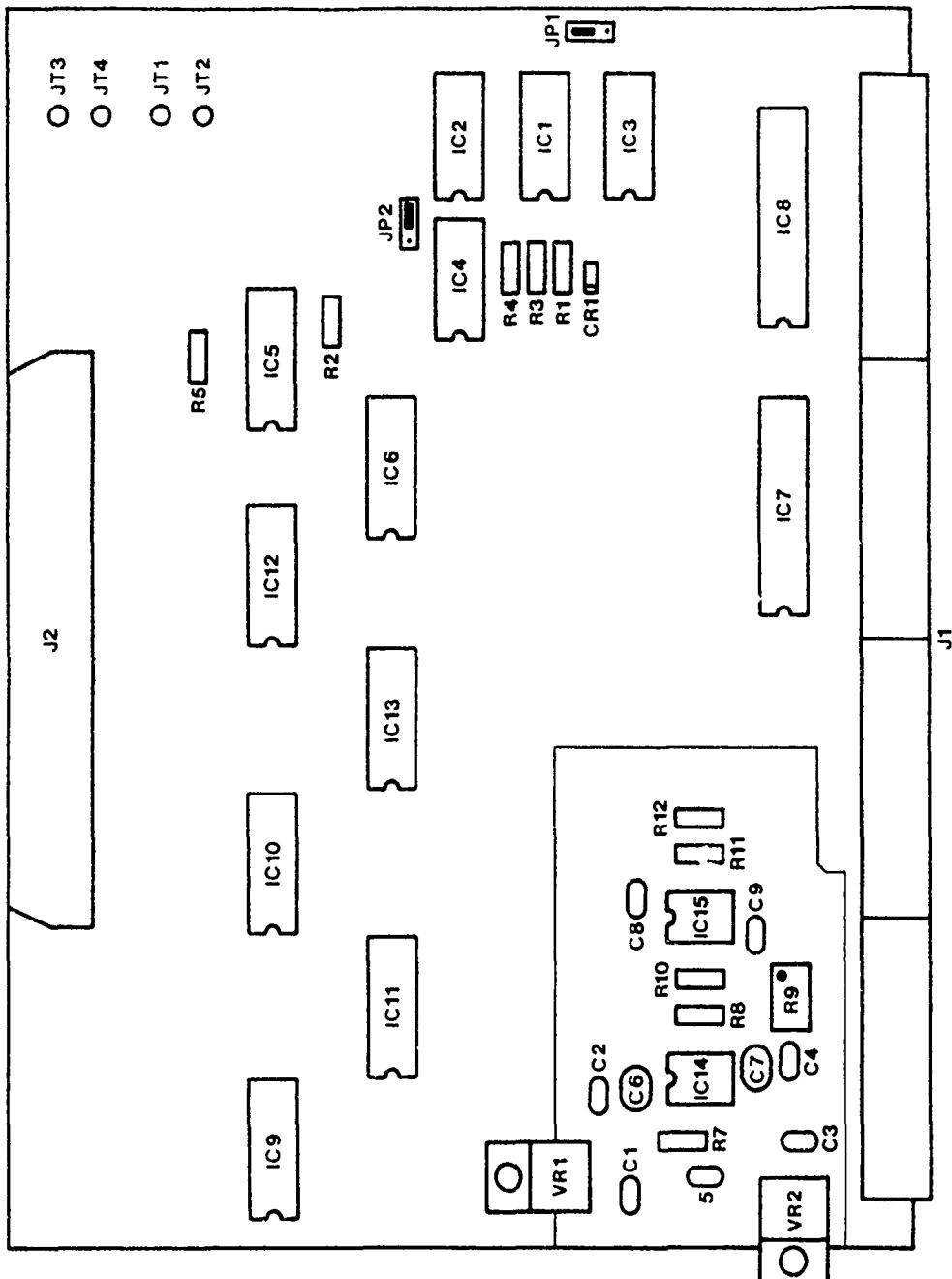
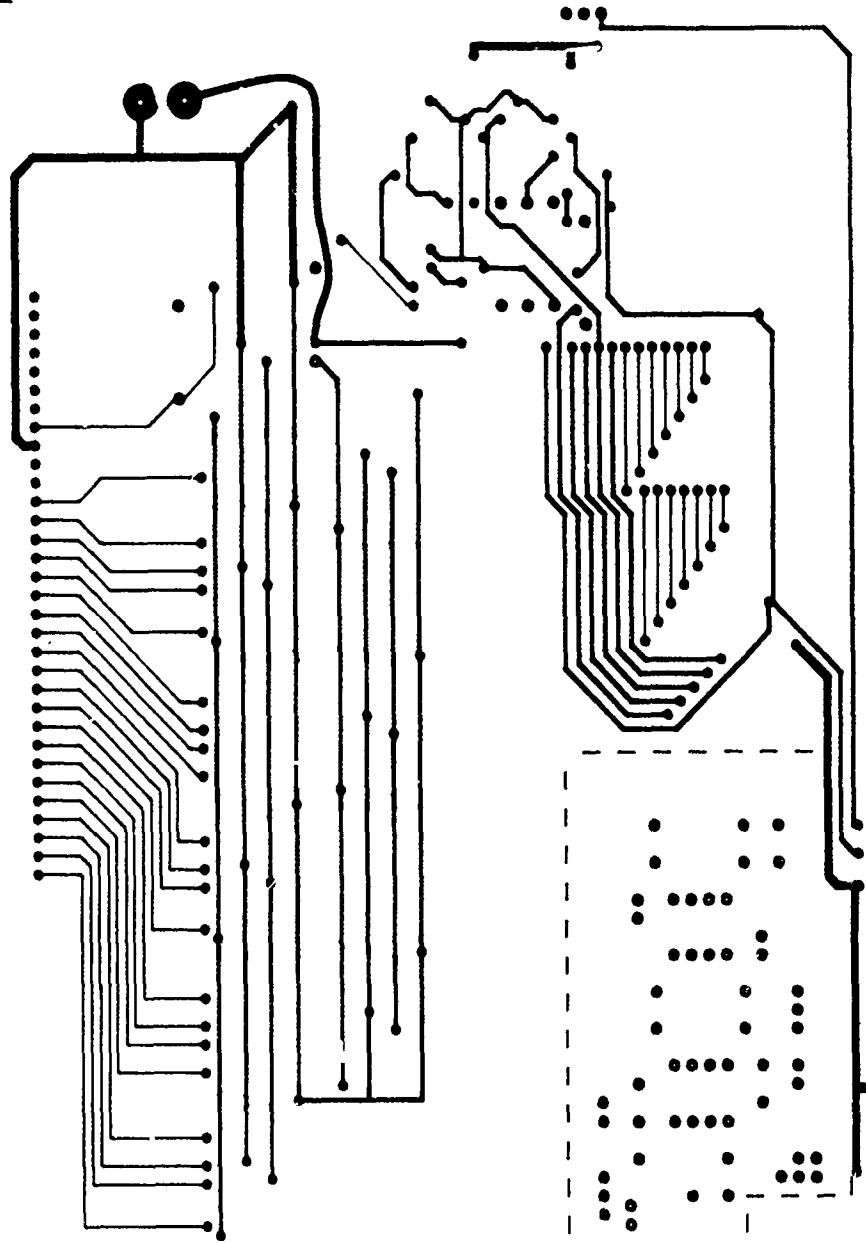


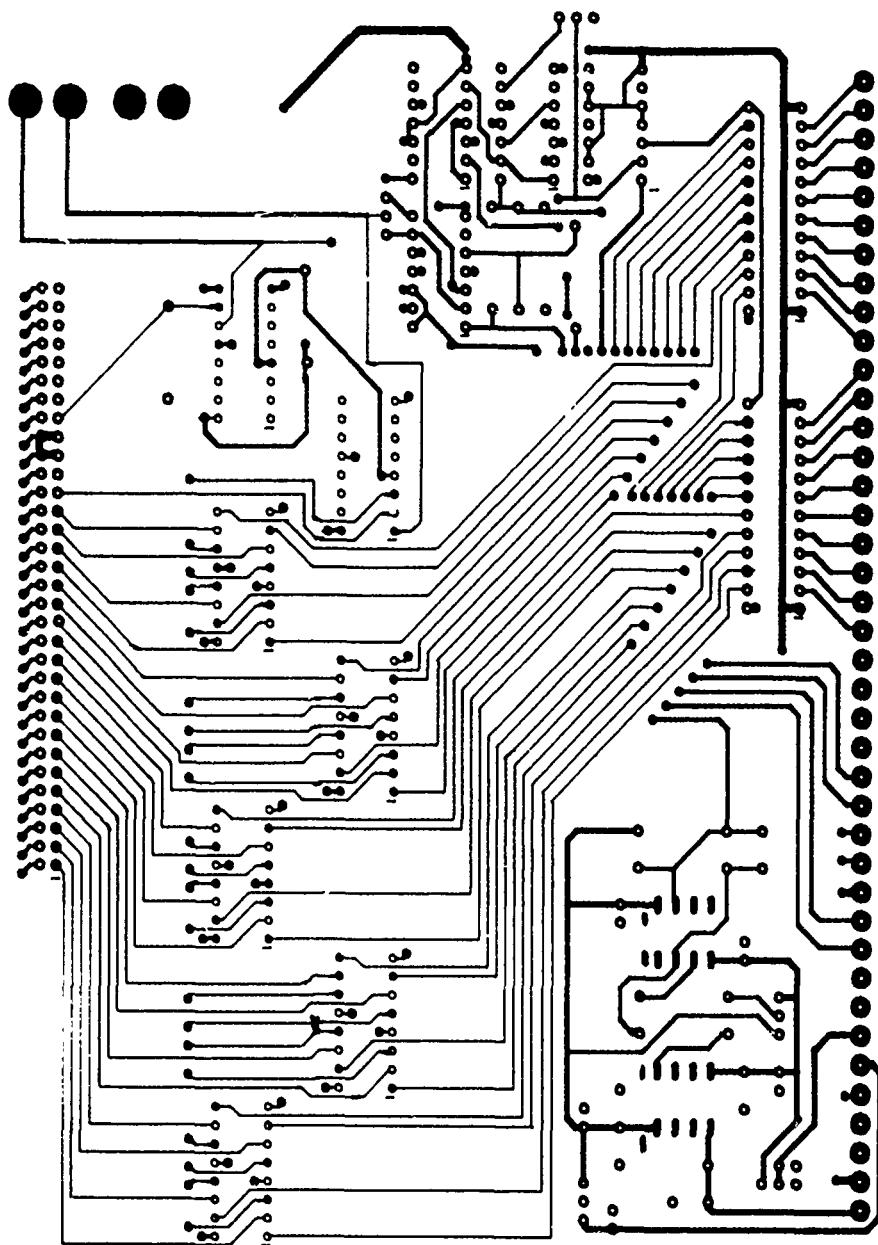
Figure 7: Latch Card Component Layout

TITLE		FILENAME		BLANK		PLT		UDRI	
FIGURE 7		FILEDATE		07-Jul-1989		FILETIME		University of Dayton	
SHEET 1 of 1		DESIGNED BY		M.J.G		SPF		Research Institute	
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Electrical Computer Department, University of Dayton									



<b>LATCH CARD ARTWORK (COMPONENT SIDE)</b>		FILENAME: BLANK PLT	—UDRI—
FILE DATE	07-JUL-1983	FILE TIME	07 49 06
FILE BY	MIG	DESIGNER	MIG
FILE NUMBER	1	FILE NUMBER	1
FILE NUMBER	8	FILE NUMBER	8
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University of Dayton Research Institute Electronics Computer Development Laboratory			

Figure 8: Latch Card Artwork (Component Side)



TITLE		LATCH CARD ARTWORK (SOLDER SIDE)		FILENAME	BLANK_PLT
				FILEDATE	07-Jul-1989
FIGURE	9	Sheet 1 of 1	DESIGNER	MG	DRAWN BY
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University of Dayton Research Institute Electronic Computer Development Division		UDARI			

Figure 9: Latch Card Artwork (Solder Side)

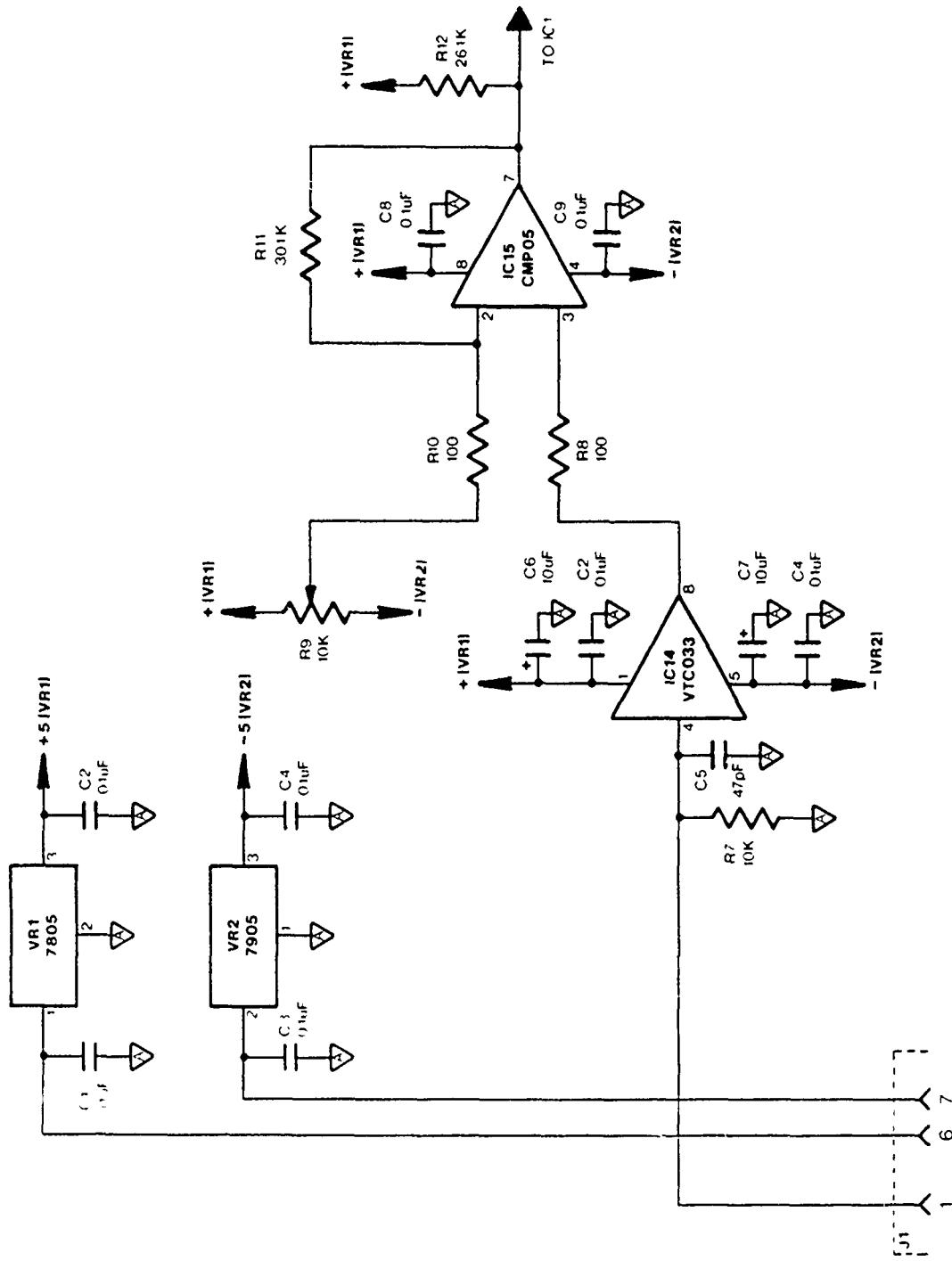


Figure 10a: Latch Card Schematic Diagram (1 of 3)

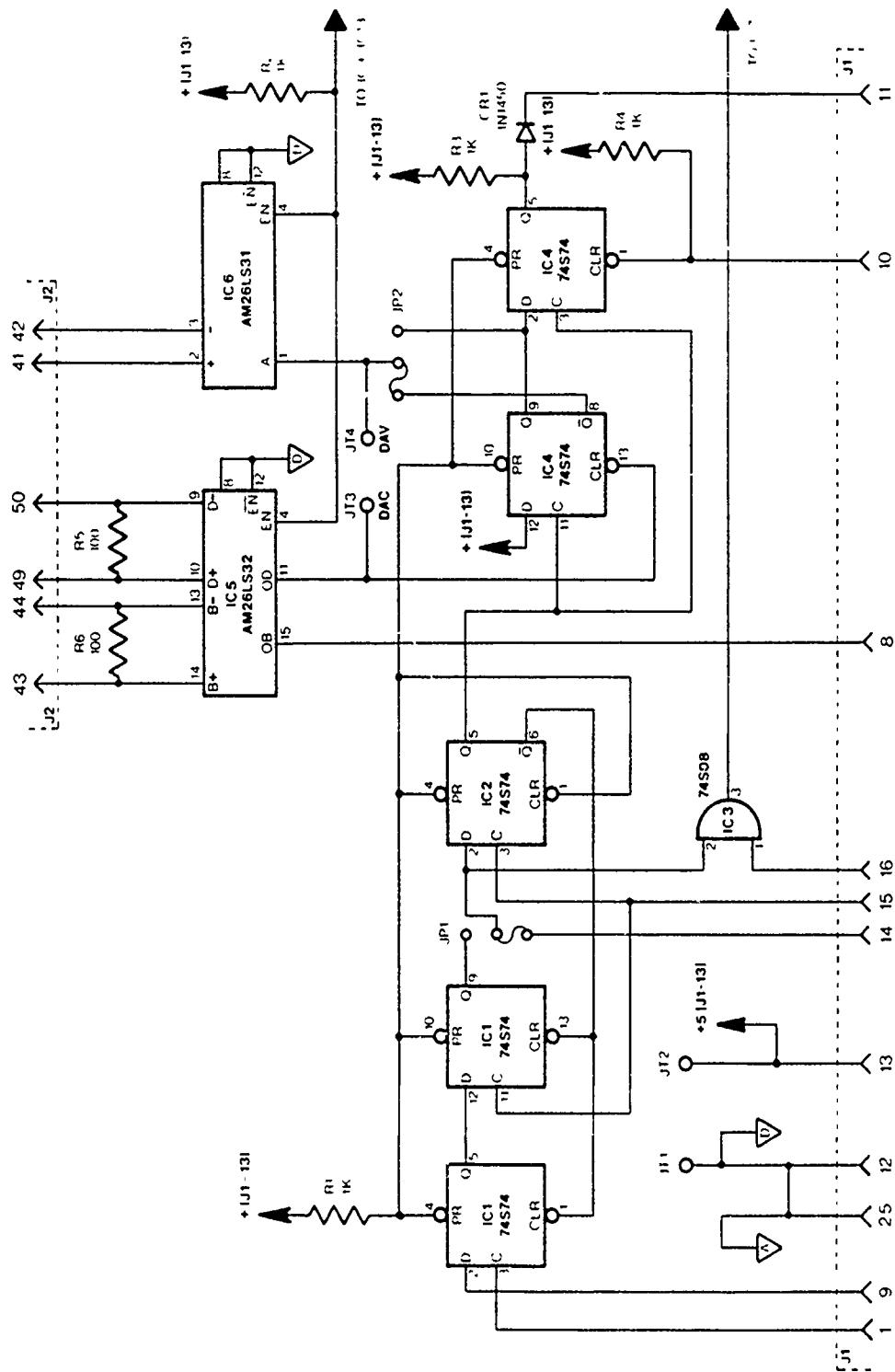
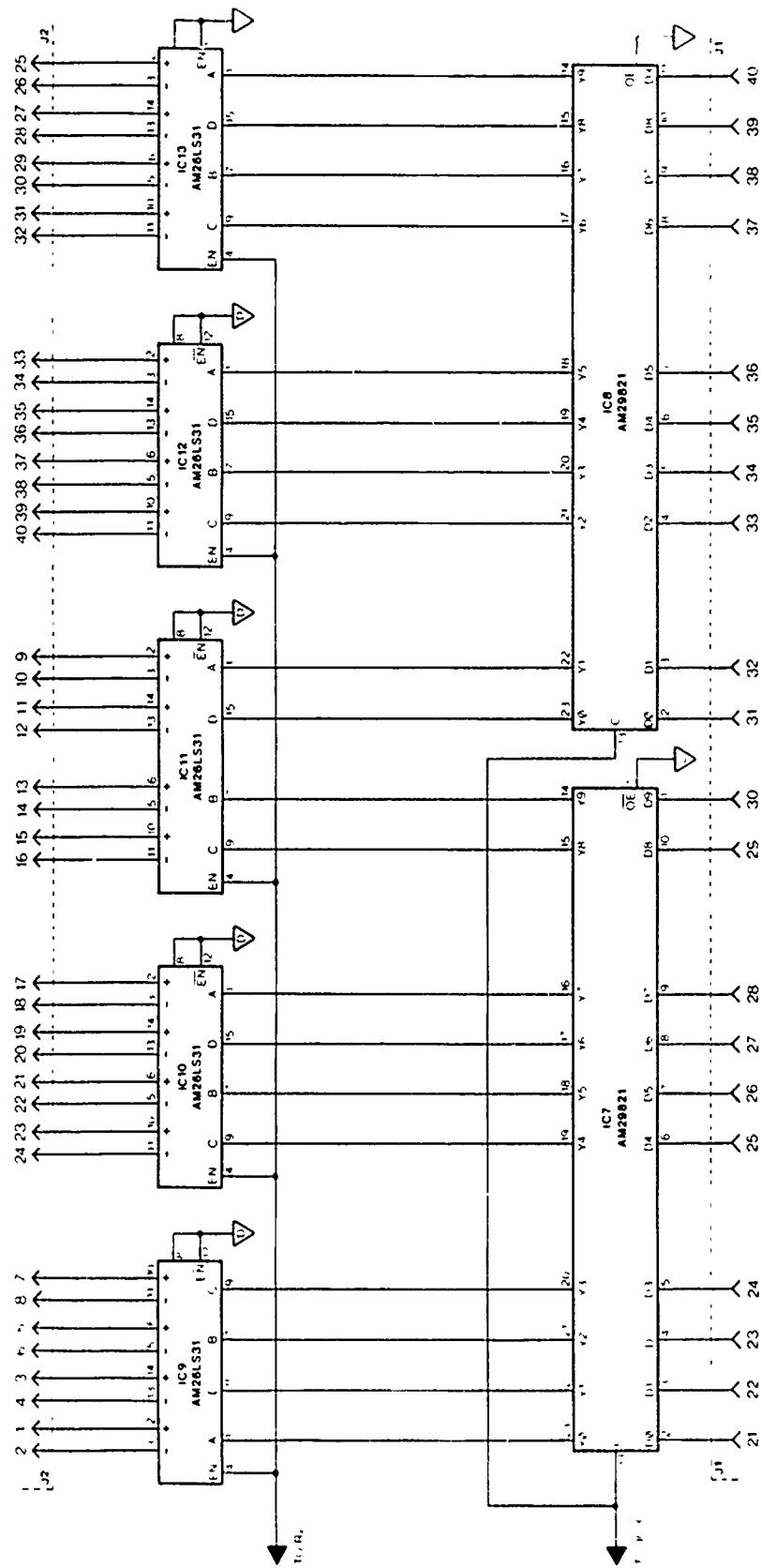


Figure 10b: Latch Card Schematic Diagram (2 of 3)

<b>LATCH CARD SCHEMATIC DIAGRAM (2 OF 3)</b>			<b>UDAI</b>		
<b>TITLE</b>	<b>DESIGNER</b>		<b>DRAWN BY</b>	<b>FILENAME</b>	<b>FILEDATE</b>
10b	Spec 2 or 3	JMA	SPF	BLANK PLT	07-Jul-1989
<b>DATE</b>	<b>DATE</b>		<b>DATE</b>	<b>DATE</b>	
© Copyr. 1989	University of Dayton Research Institute		07.49.06	ESCO - Instrumental Services	



LATCH CARD SCHEMATIC DIAGRAM  
(3 OF 3)

UDRI

University of Dayton  
Research Institute

Project 1

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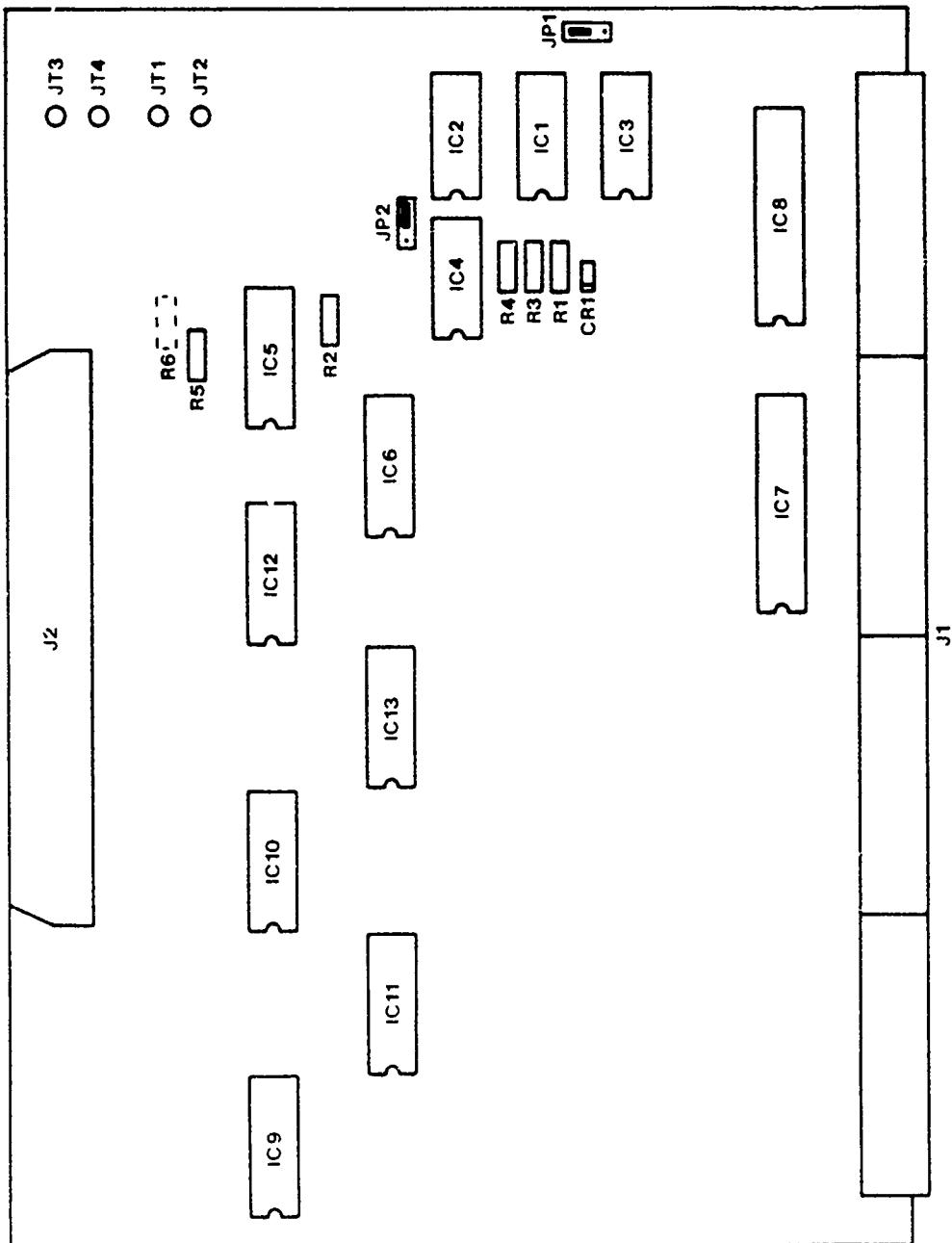
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**Latch Card Parts List**

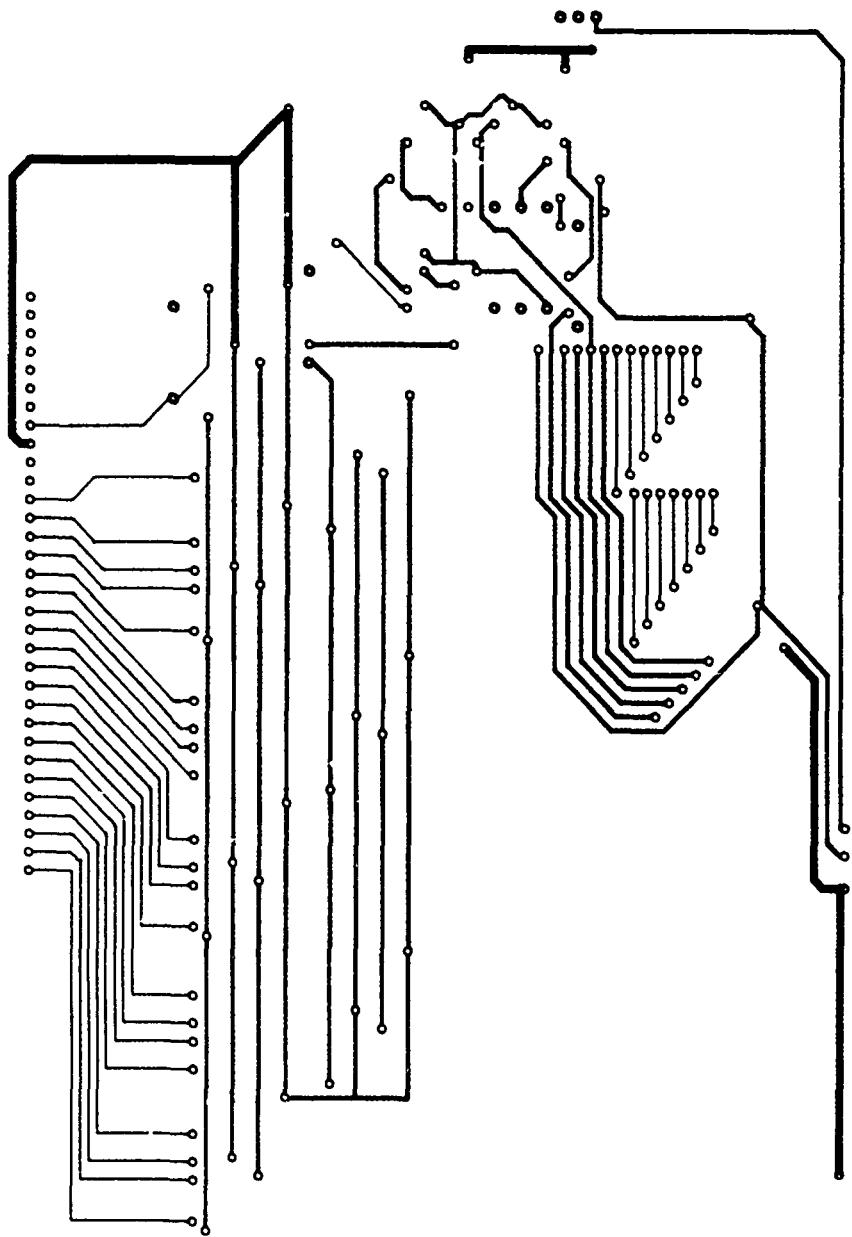
Part Number	Description
R1 - R5	1 KOhm
R7, 10	KOhm
R8, R10	100 Ohm
R11	30.1 KOhm
R12	26.1 KOhm
R9	10KOhm Trimpot
C1 - C4, C8, C9	0.1 uF
C5	47 pF
C6, C7	10 uF Tantalum
IC1, IC2, IC4	74S74
IC3	74S08
IC5	Am26LS32
IC6, IC9 - IC13	Am26LS31
IC7, IC8	Am29821
IC14	VTC033
IC15	CMP05
VR1	7805
VR2	7905
CR1	1N4150
J1	Molex .156 10 position (x4)
J2	Ansley Blue Macs 50 pin male

Table 1: Latch Card Parts List



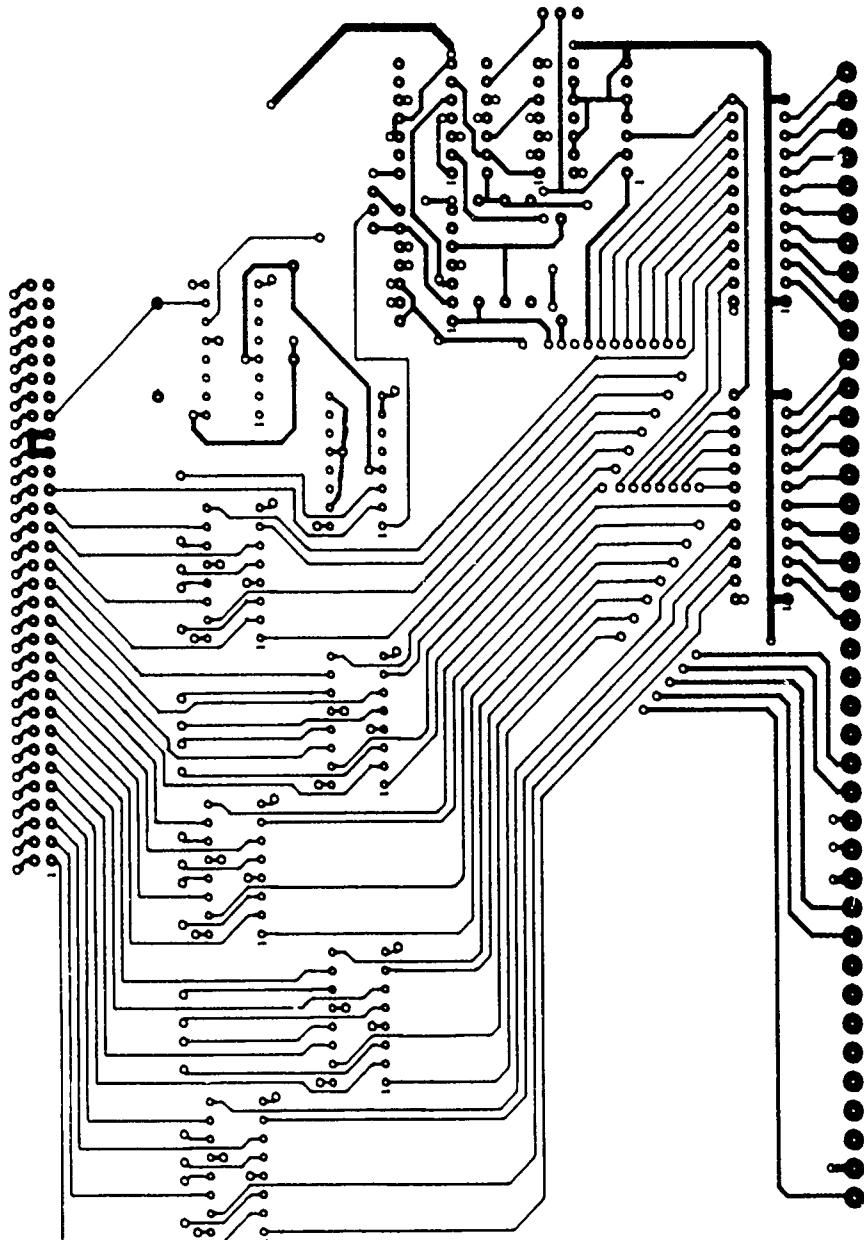
Title 1PPR LATCH CARD COMPONENT LAYOUT		Picture BLANK PLT		UDRI	
Figure 11	Sheet 1 of 1	Designer MJG	Date 6/20/89	Printed 07-12-1989	University of Dayton Research Institute Instrumentation, Control, and Robotics Laboratory
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Figure 11: 1PPR Latch Card Component Layout



<b>UDRI</b>	
University of Dayton Research Institute Electrical-Computer Engineering Laboratory	
<b>1PPR Latch Card Artwork (Component Side)</b>	
FIGURE 12	BLANK PLT
FIGURE 12	07-Jul-1989
DESIGNED by M.J.G	DRAWN BY M.J.G
FILETYPE 07-49-06	
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Figure 12: 1PPR Latch Card Artwork (Component Side)



1PPR LATCH CARD ARTWORK (SOLDER SIDE)		RELEASE BLANK PLT	UDRI
FILE	1PPR LATCH CARD	RELEASE DATE	University of Dayton
NAME		07-01-1989	Research Institute
DESIGNER	M.J.G.	DESIGNER	Electronic Computer Development Laboratory
DATE	Sheet 1 of 1	DATE	EDC
PLATE	13	PLATE	17-25-05
©	Copyright 1989	©	University of Dayton Research Institute ECD Laboratory

Figure 13: 1PPR Latch Card Artwork (Solder Side)

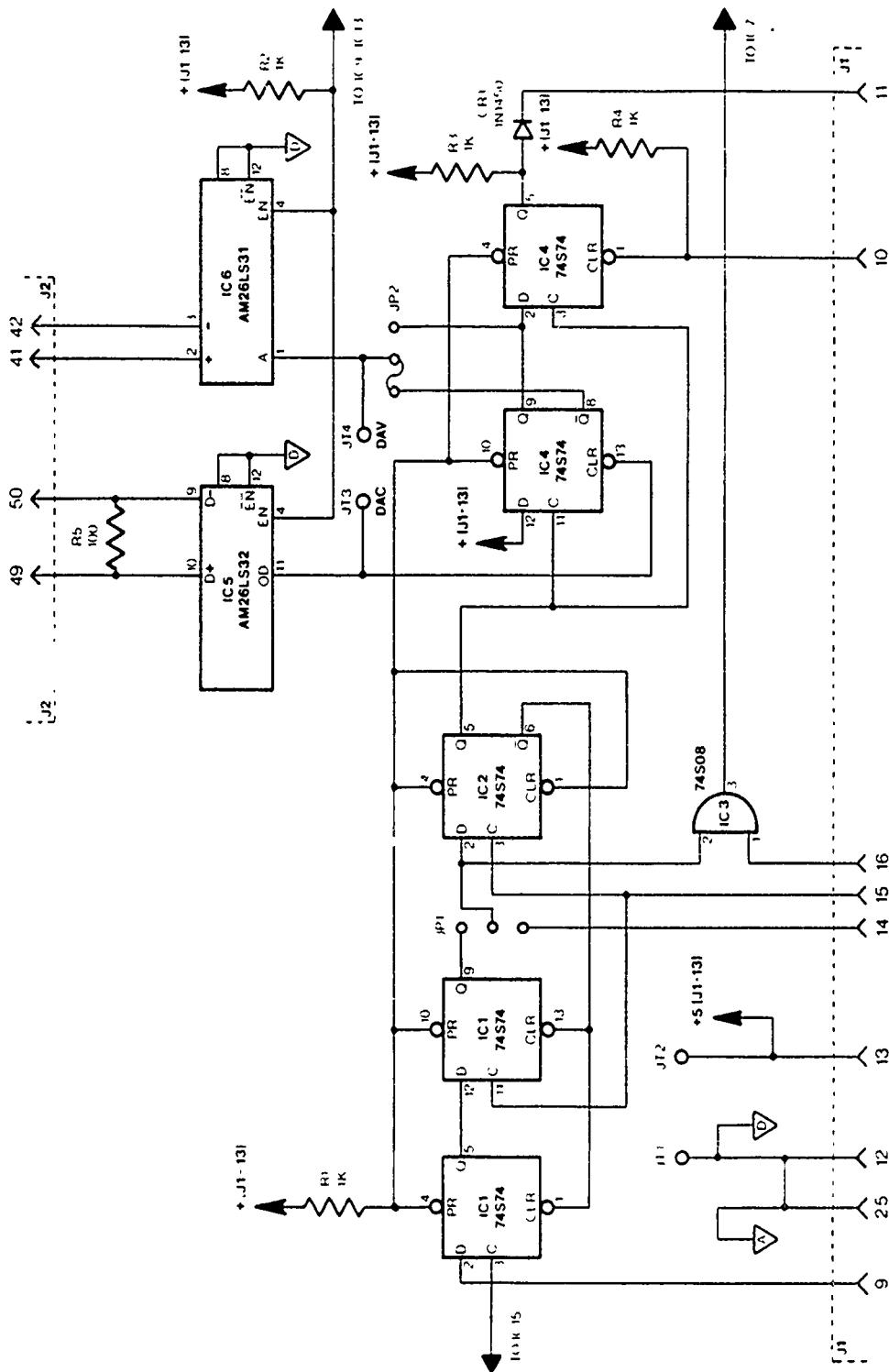


Figure 14a: 1PPR Latch Card Schematic Diagram (1 of 2)

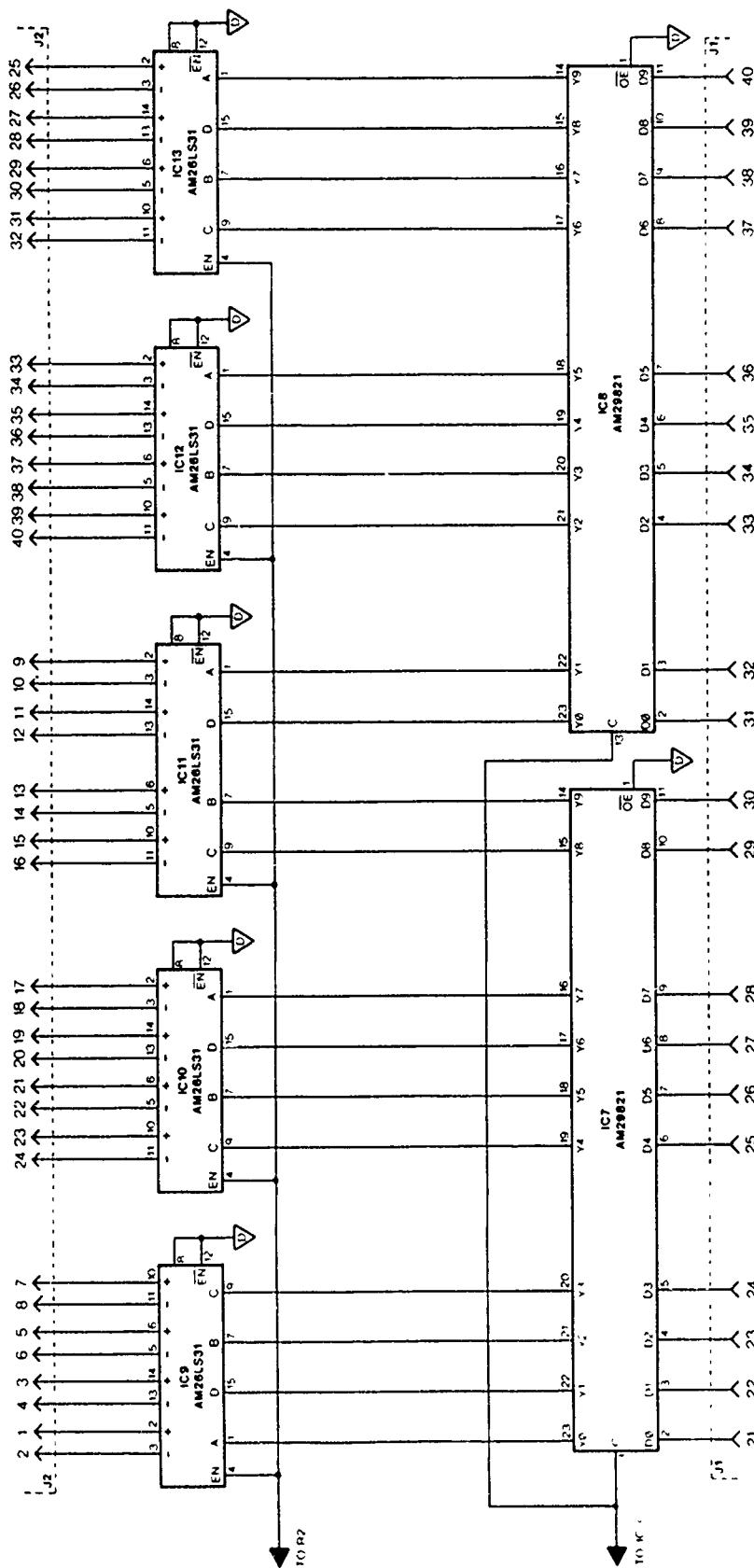


Figure 14b: 1PPR Latch Card Schematic Diagram (2 of 2)

TITLE		1PPR LATCH CARD SCHEMATIC	
FIGURE		2 OF 2	
FIGURE		BLANK PL1	
FIGURE		07-JUL-1989	
14b	2 or 2	DESIGNER	JMA
		DRAWN BY	SpF
		DATE	07 49 06
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UDRI			
University of Dayton Research Institute Electronic Computer Development Laboratory			

1PPR Latch Card Parts List

Part Number	Description
R1 - R6	1 KOhm
IC1, IC2, IC4	74S74
IC3	74S08
IC5	Am26LS32
IC6, IC9 - IC13	Am26LS31
IC7, IC8	Am29821
CR1	1N4150
J1	Molex .156 10 position (x4)
J2	Ansley Blue Macs 50 pin male

Table 2: 1PPR Latch Card Parts List

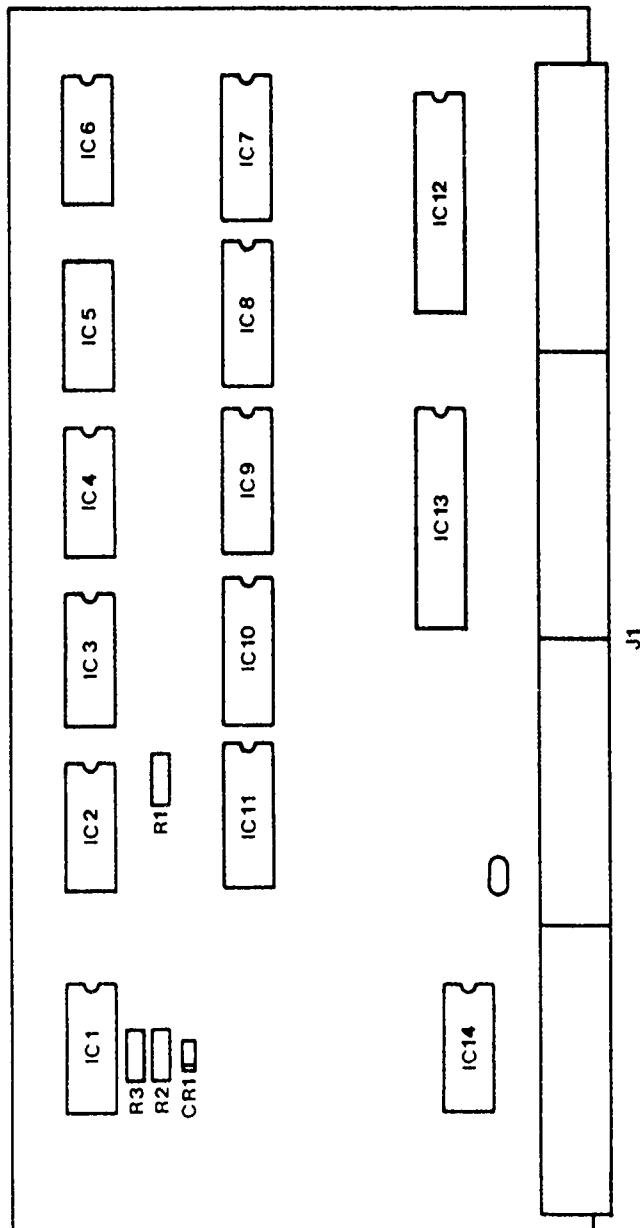
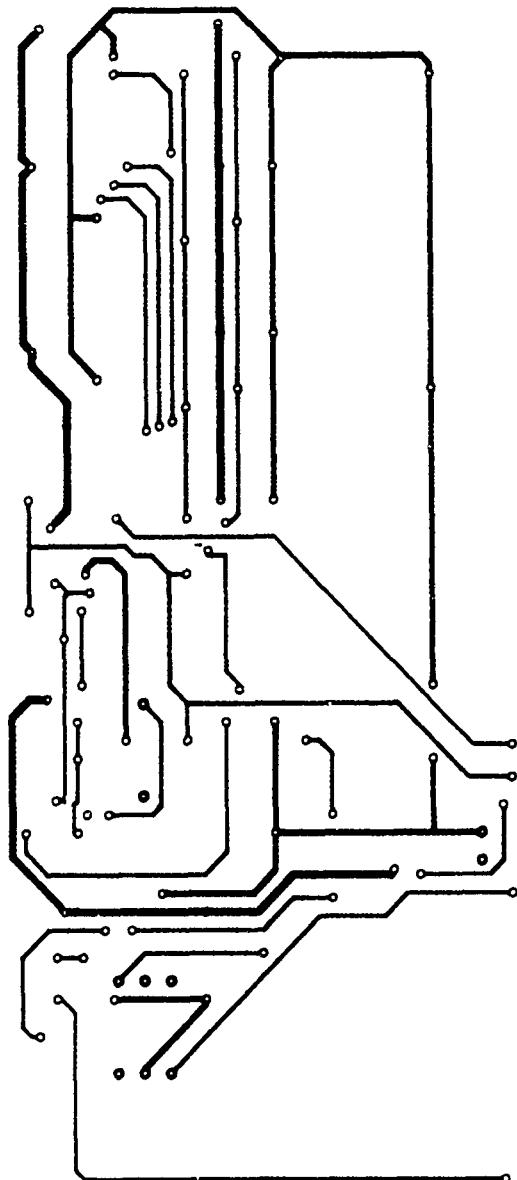


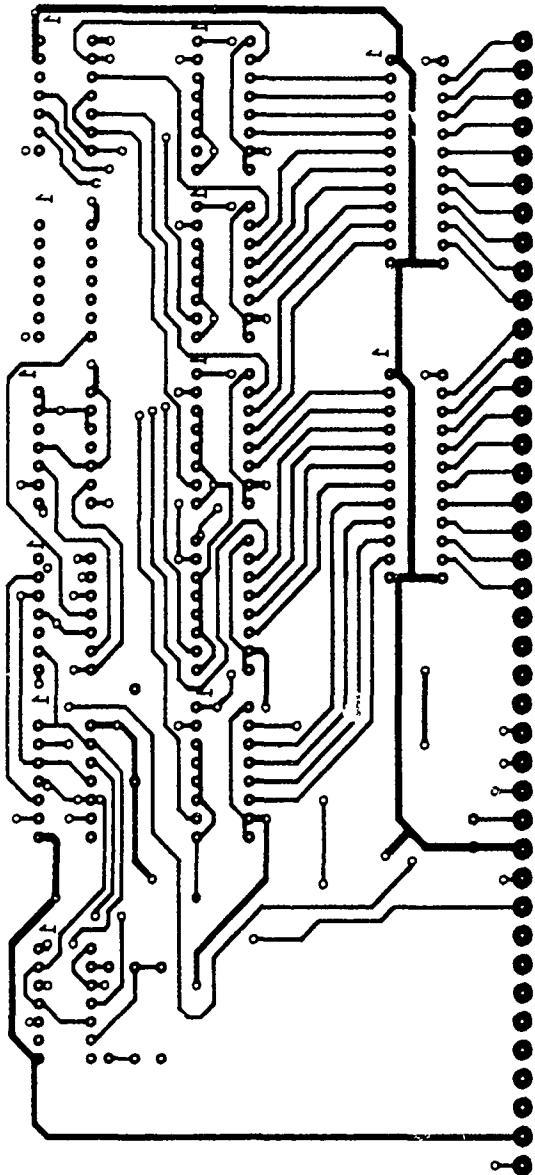
Figure 15: Counter Card Component Layout

TITLE			COUNTER CARD COMPONENT LAYOUT		FILENAME	BLANK	PLT	UDRI
FIGURE	Sheet 1 of 1	DESIGNER	M. -	DRAWN BY	DATE	07-JUL-1989	University of Dayton Research Institute Electrical Engineering Laboratory	
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TITLE		COUNTER CARD ARTWORK		-UDRI-	
		(COMPONENT SIDE)			
FIGURE		FILENAME BLANK PLT		University of Dayton	
16		FILEDATE 07 - Jul - 1989		Research Institute	
Sheet 1 of 1		DESIGNER	M.J.G.	FILETIME	07 49 06
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Figure 16: Counter Card Artwork (Component Side)



TITLE		COUNTER CARD ARTWORK (SOLDER SIDE)		FILENAME		BLANK_PLT	
FIGURE		17		FILEDATE	C7-JUL-1989		
SHEET		1 of 1		DRAWN BY	M.J.G		
DESIGNER				FILETIME	07:49:06		
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University of Dayton Research Institute Electrical Computer Engineering Department							

Figure 17: Counter Card Artwork (Solder Side)

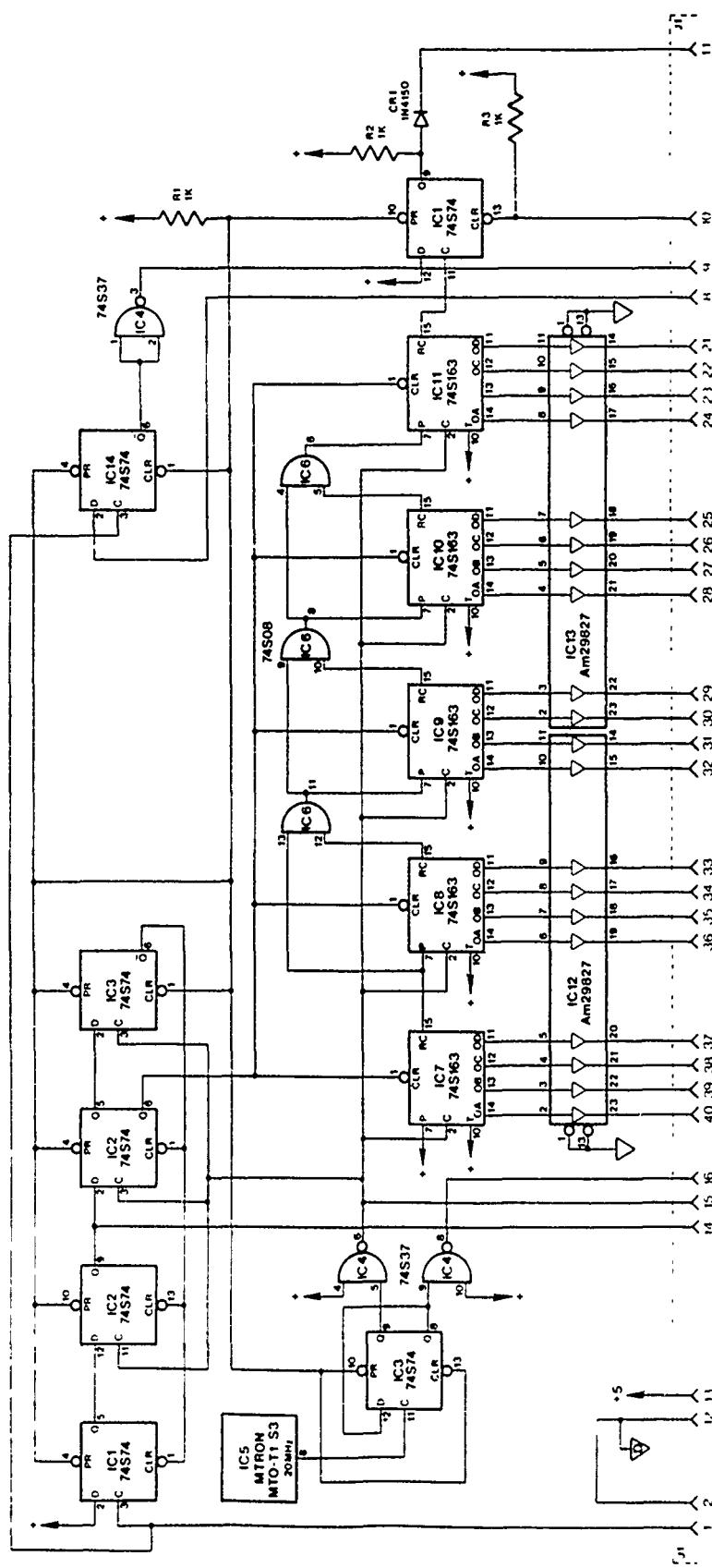


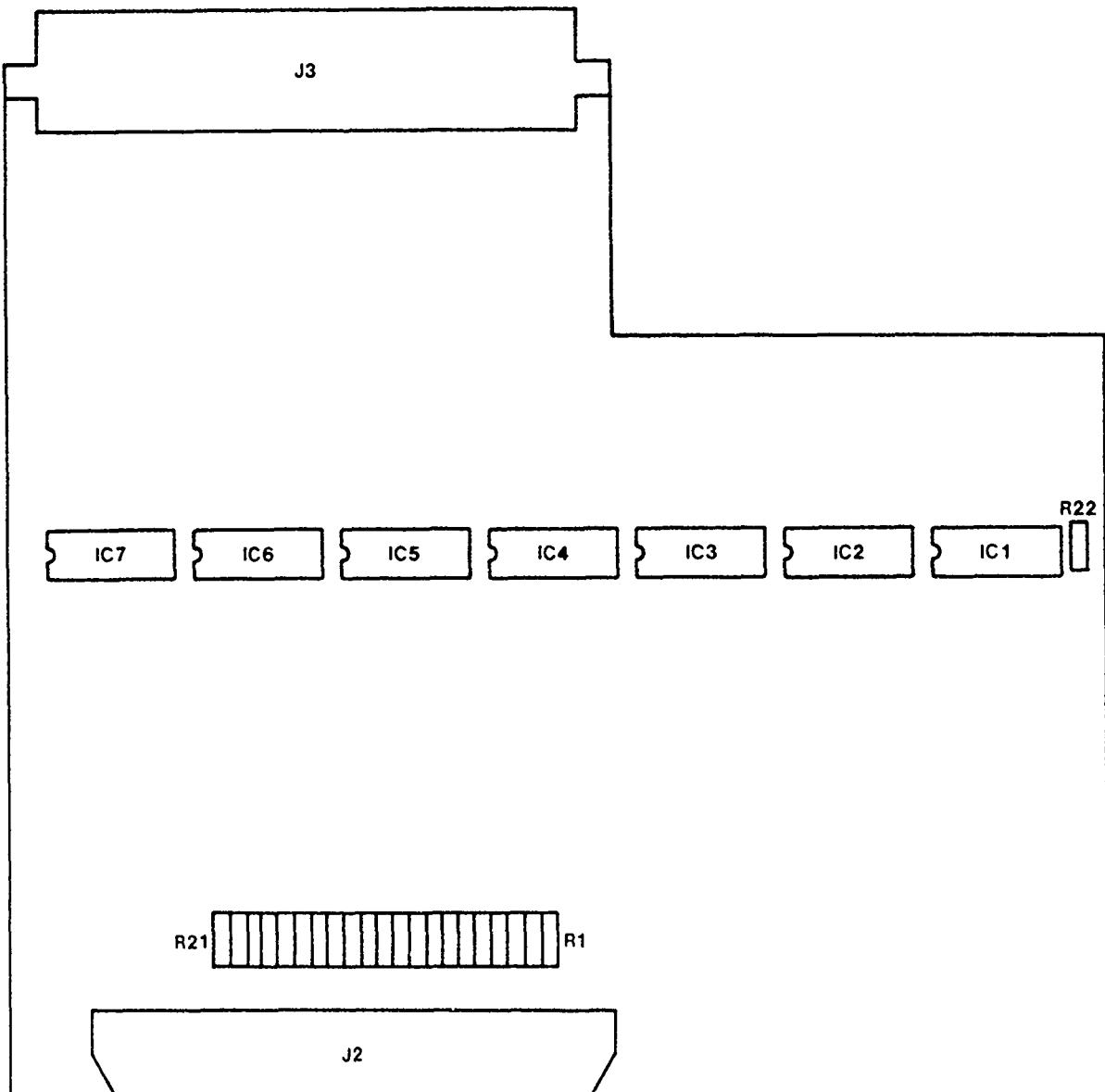
Figure 18: Counter Card Schematic Diagram

<b>COUNTER CARD SCHEMATIC</b>		<b>BLANK PLT</b>
		<b>FILEDATE</b> 07-Jul-1989
<b>FILE#</b> 18	<b>DESIGNED</b> 1 or 1	<b>DRAWN BY</b> JMA
		<b>FILETIME</b> 07 49. 06
<b>© Copyright 1989, University of Dayton Research Institute, ESCO Laboratory</b>		
<b>UDRI</b> —		<b>University of Dayton</b> <b>Research Institute</b> <small>Electrical &amp; Computer Development Laboratory</small>

Counter Card Parts List

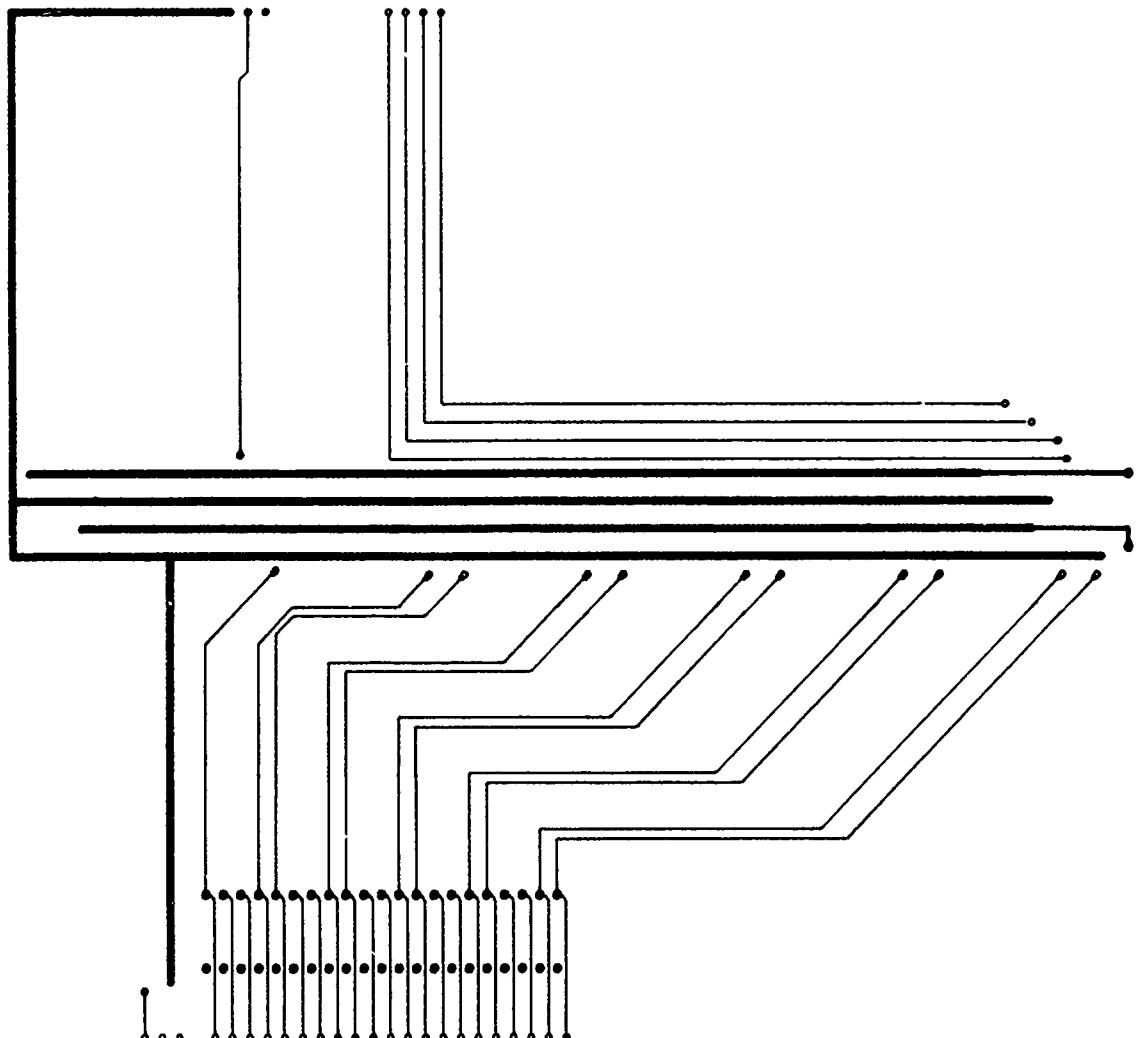
Part Number	Description
R1 - R3	1 KOhm
IC1 - IC3	74S74
IC4	74S37
IC5	MTO-T1-S3 (Mtron)
IC6	74S08
IC7 - IC11	74S163
IC12, IC13	AM29827
CR1	1N4150
J1	Molex .156 10 position (x4)

Table 3: Counter Card Parts List



TITLE RECEIVER AND 1PPR RECEIVER CARDS COMPONENT LAYOUT				FILENAME BLANK PLT	UDRI University of Dayton Research Institute Electronic & Computer Development Laboratory
FIGURE 19	SHEET 1 OF 1	DESIGNER M.J.G	DRAWN BY SPF	FILEDATE 07-Jul-1989	
FILETIME 07 49 06 © Copyright 1989. University of Dayton Research Institute ESCD Laboratory					

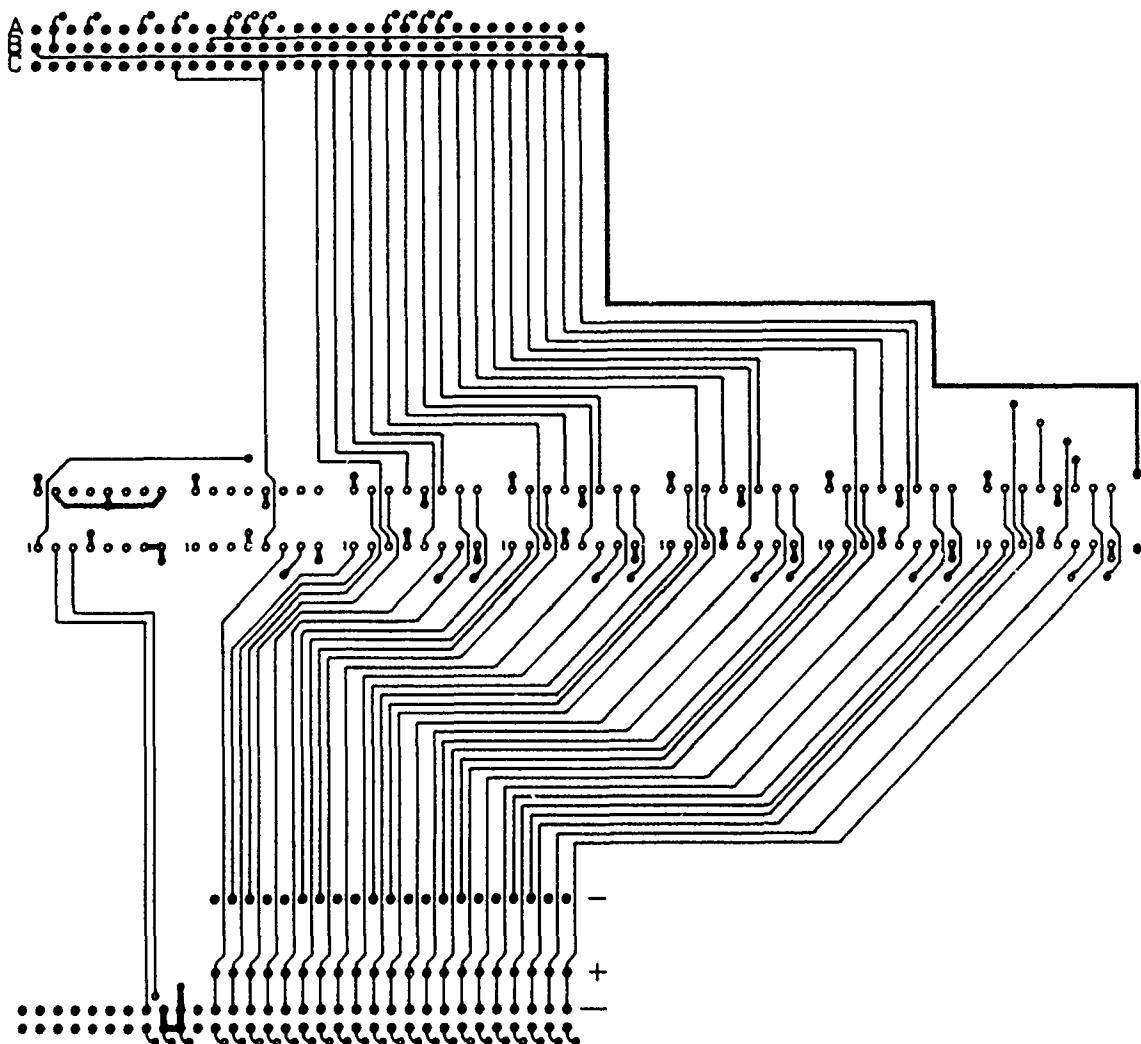
Figure 19: Receiver and 1PPR Receiver Cards Component Layout



TITLE RECEIVER AND 1PPR RECEIVER CARDS ARTWORK (COMP. SIDE)			FILENAME RECEVR_PLT	—UDRI—
FIGURE 20	DESIGNER MJG	DRAWN BY "B"	CREATED 07/16/1989	University of Dayton Research Institute Electronic & Computer Development Laboratory
SHEET 1 OF 1			UPDATED 07/19/06	

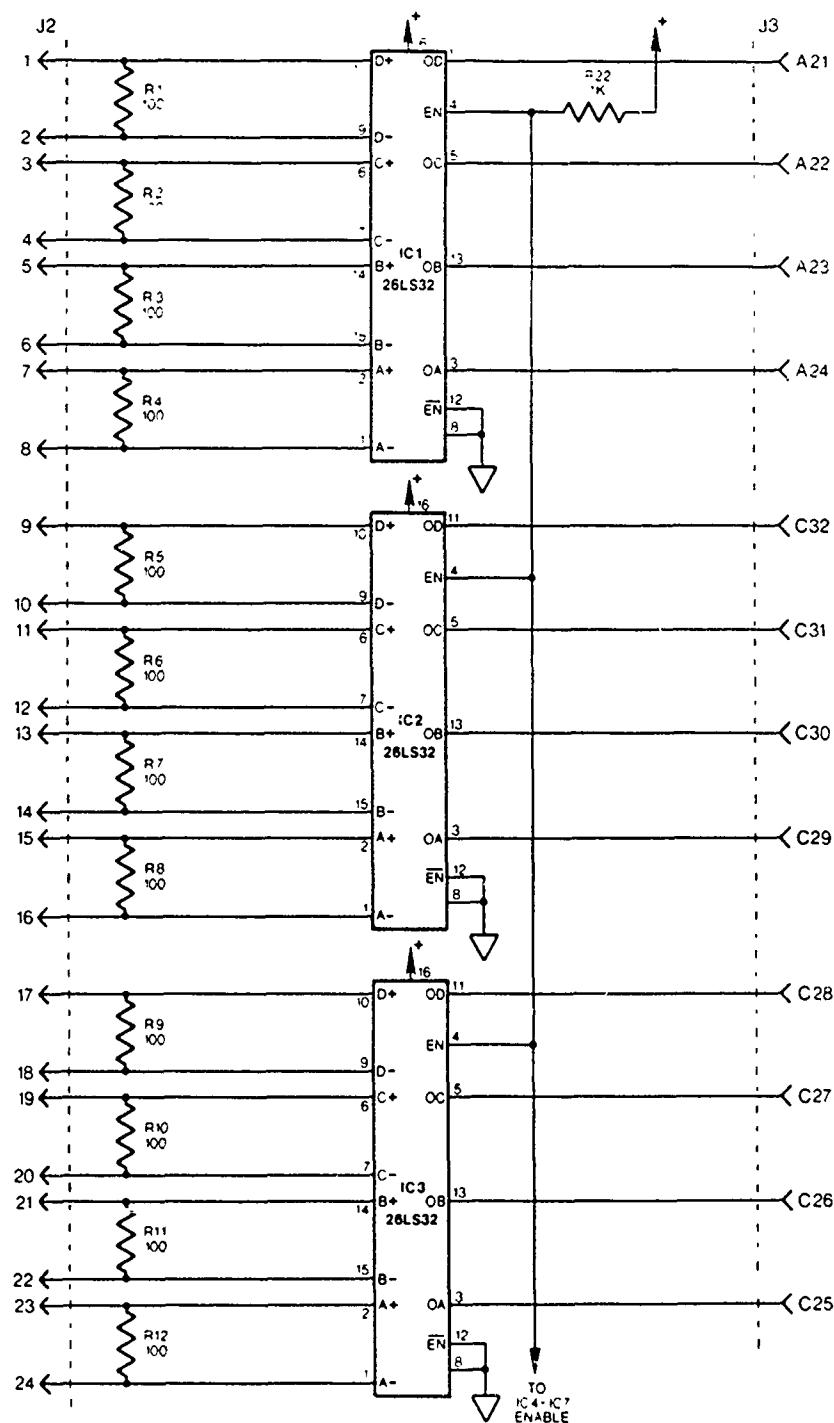
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Figure 20: Reciever and 1PPR Receiver Cards Artwork (Comp. Side)



TITLE RECEIVER AND 1PPR RECEIVER CARDS ARTWORK (SOLDER SIDE)				FILENAME BLANK.PLT
FIGURE 21				FILEDATE 07-Jul-1989
FIGURE 21	SHEET 1 of 1	DESIGNER MUG	DRAWN BY	FILETIME 07 49 06
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Figure 21: Receiver and 1PPR Receiver Cards Artwork (Solder Side)



TITLE RECEIVER CARD SCHEMATIC DIAGRAM (1 OF 2)				FILENAME BLANK.PLT	UDRI
FIGURE 22a	SHEET 1 OF 2	DESIGNER JMA	DRAWN BY SPF	FILEDATE 07 JUL 1989	University of Dayton Research Institute Electronic & Computer Development Laboratory
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Figure 22a: Receiver Card Schematic Diagram (1 of 2)

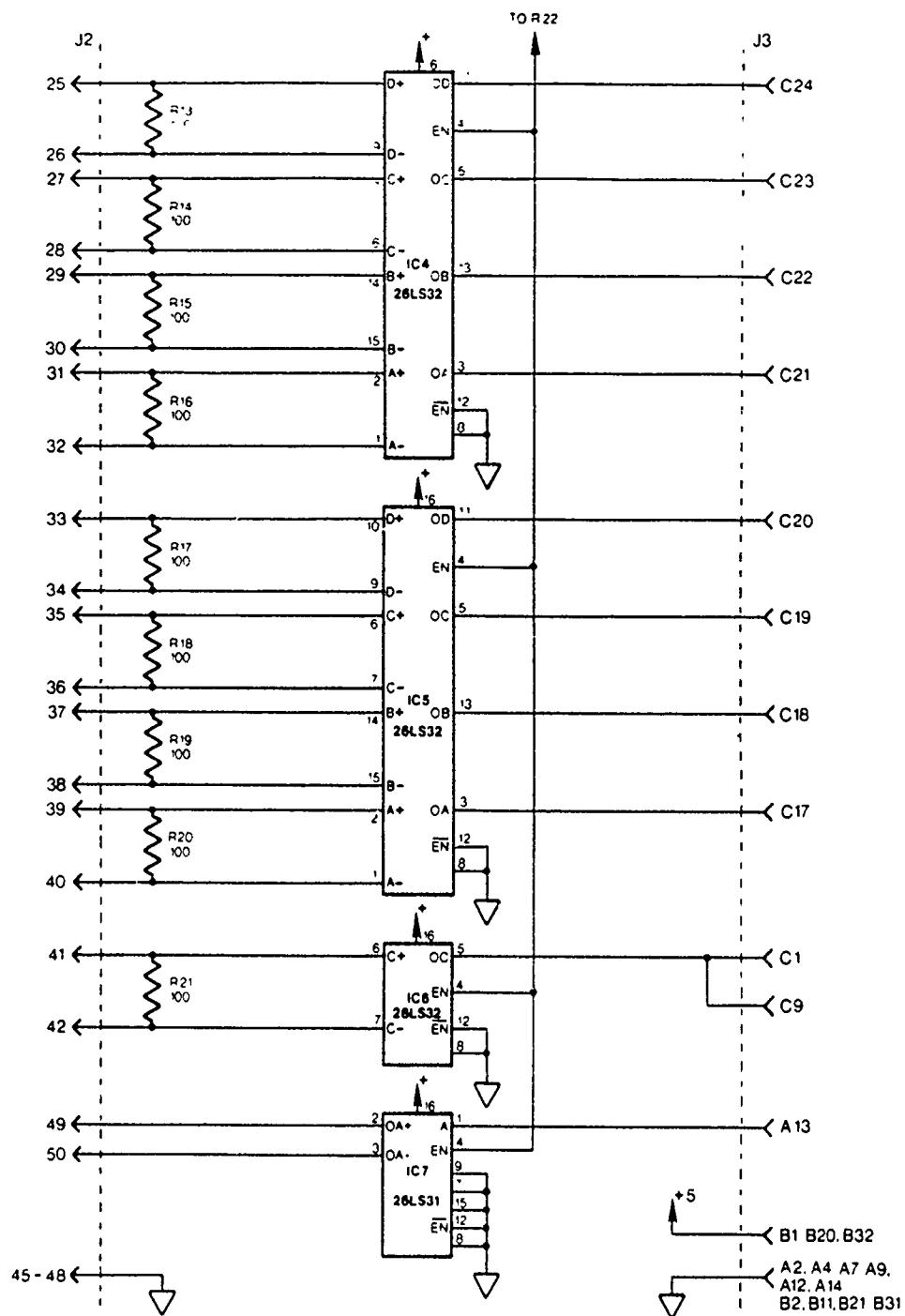
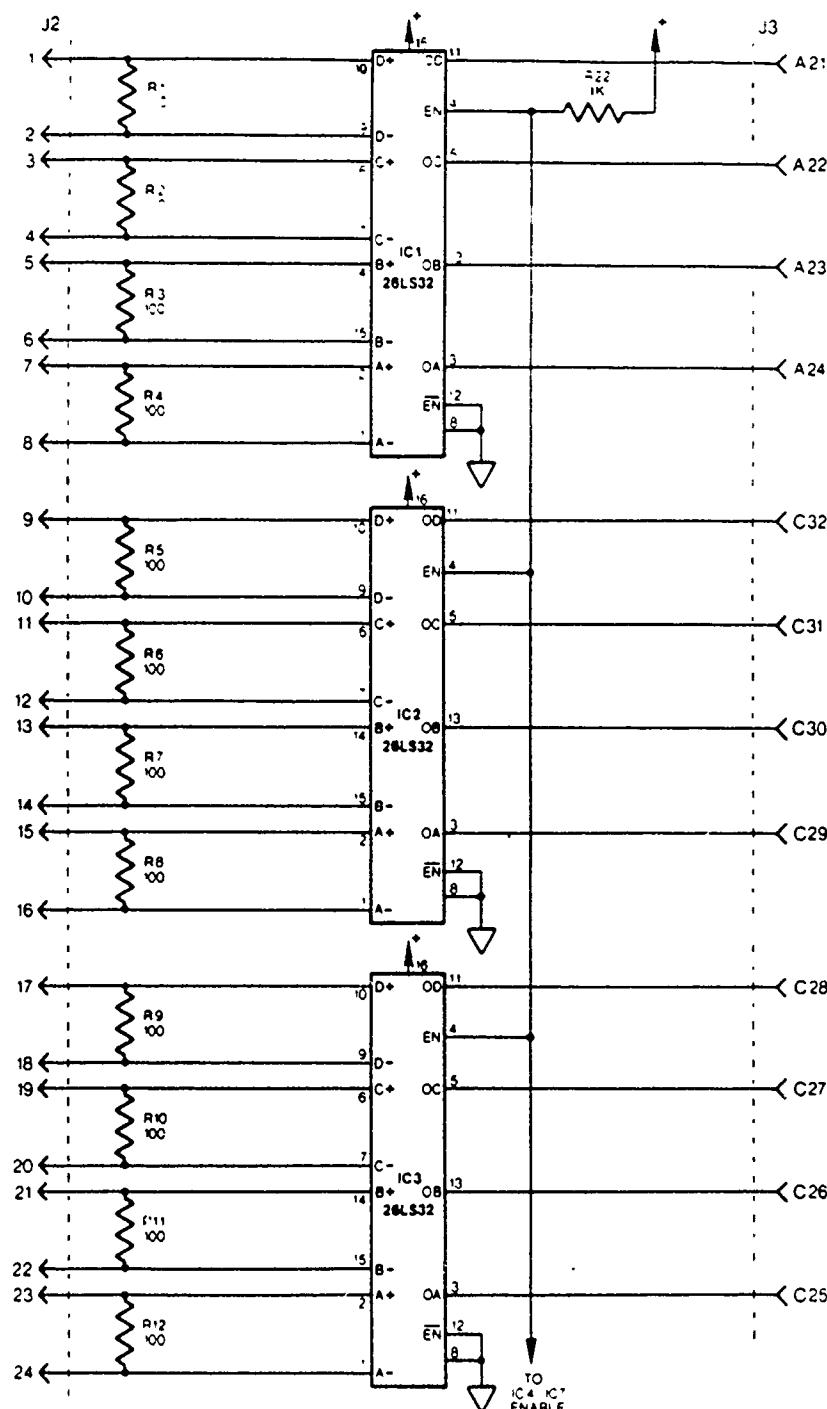


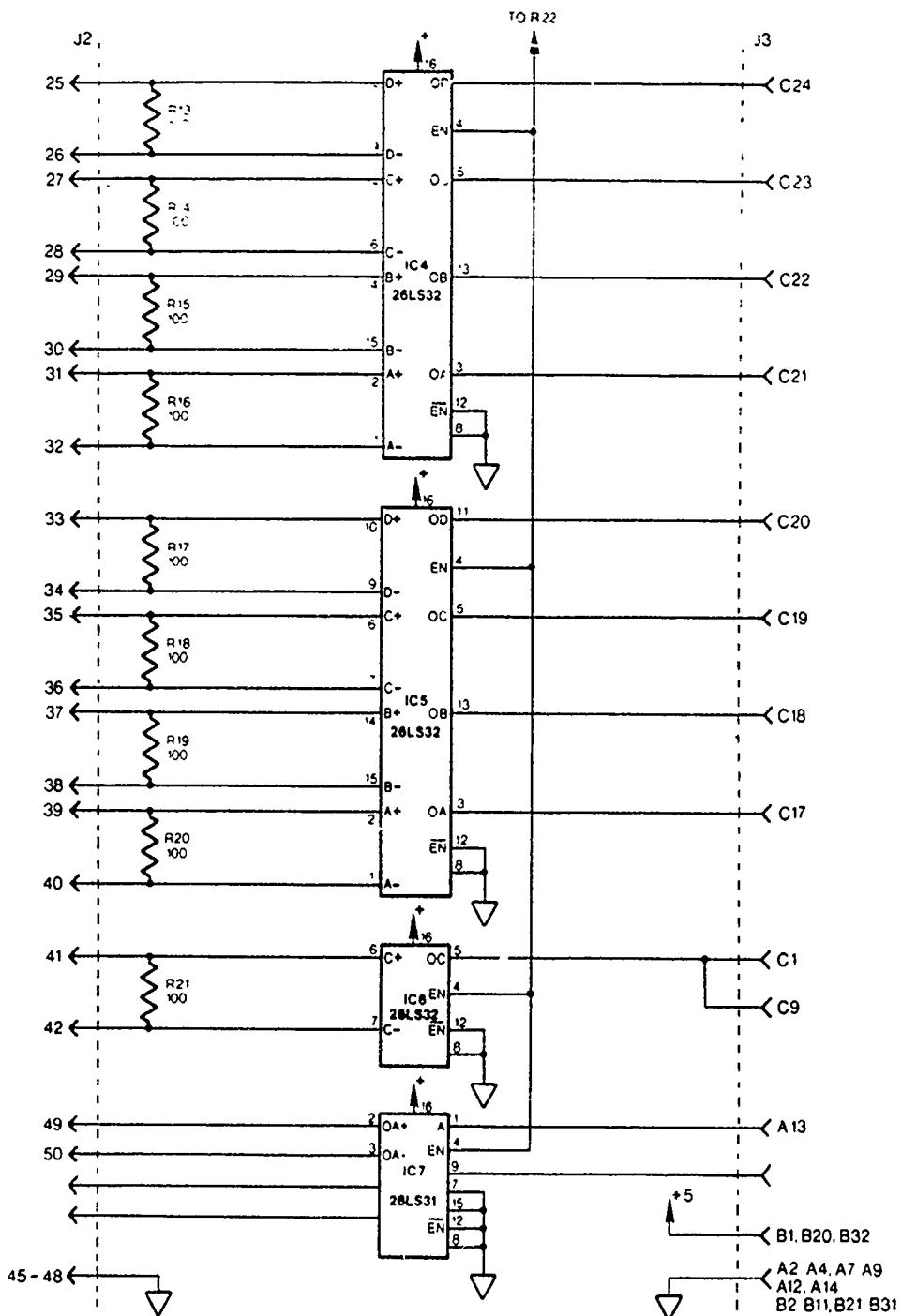
FIGURE	RECEIVER CARD SCHEMATIC DIAGRAM (2 OF 2)			FILENAME	BLANK_P11	
FIGURE	22b	Sheet 2 of 2	DESIGNER	JMA	FILEDATE	07-Jul-1989
FIGURE			DRAWN BY	SPF	FILETIME	07 49 06
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						University of Dayton Research Institute Electronic & Computer Development Laboratory

Figure 22b: Receiver Card Schematic Diagram (2 of 2)



TITLE 1PPR RECEIVER CARD SCHEMATIC DIAGRAM (1 OF 2)				FILENAME BLANK.PLT			
FIGURE 23a	1	MA	DRAWN BY JPH	DATE 07/01/1989	ENTERED BY JPH	DATE 07/19/89	UDRI University of Dayton Research Institute Electron & Computer Development Laboratory
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Figure 23a: 1PPR Receiver Card Schematic Diagram (1 of 2)



TITLE 1PPR RECEIVER CARD SCHEMATIC DIAGRAM (2 OF 2)				FILENAME BLANK PLT	UDRI University of Dayton Research Institute Electronics & Computer Development Laboratory
FIGURE 23b	SHEET 2 OF 2	DESIGNER JMA	DRAWN BY SPF	FILEDATE 07-Jul-1989	

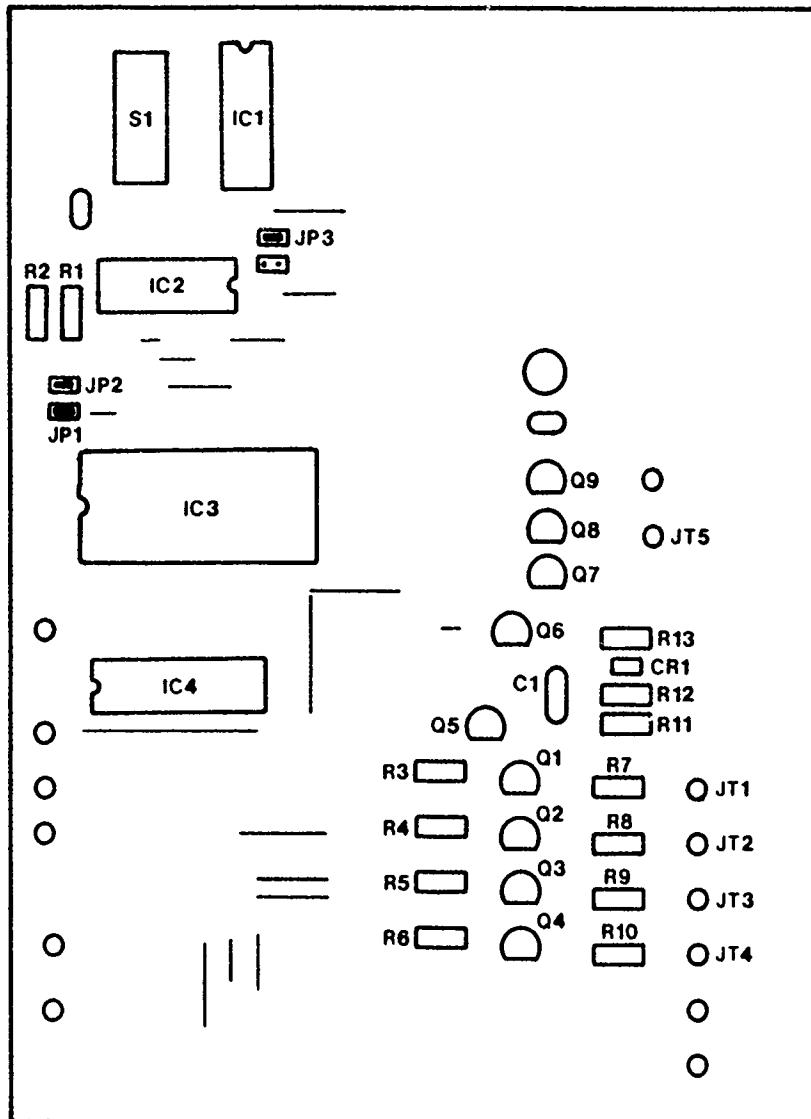
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Figure 23b: 1PPR Receiver Card Schematic Diagram (2 of 2)

**Receiver and 1PPR Receiver Cards Parts List**

<b>Part Number</b>	<b>Description</b>
R1 - R21	100 Ohm
R22	1 Kohm
IC1 - IC6	Am26LS32
IC7	Am26LS31
J2	Ansley Blue Macs 50 pin male
J3	Ansley 64 Pin DIN VME

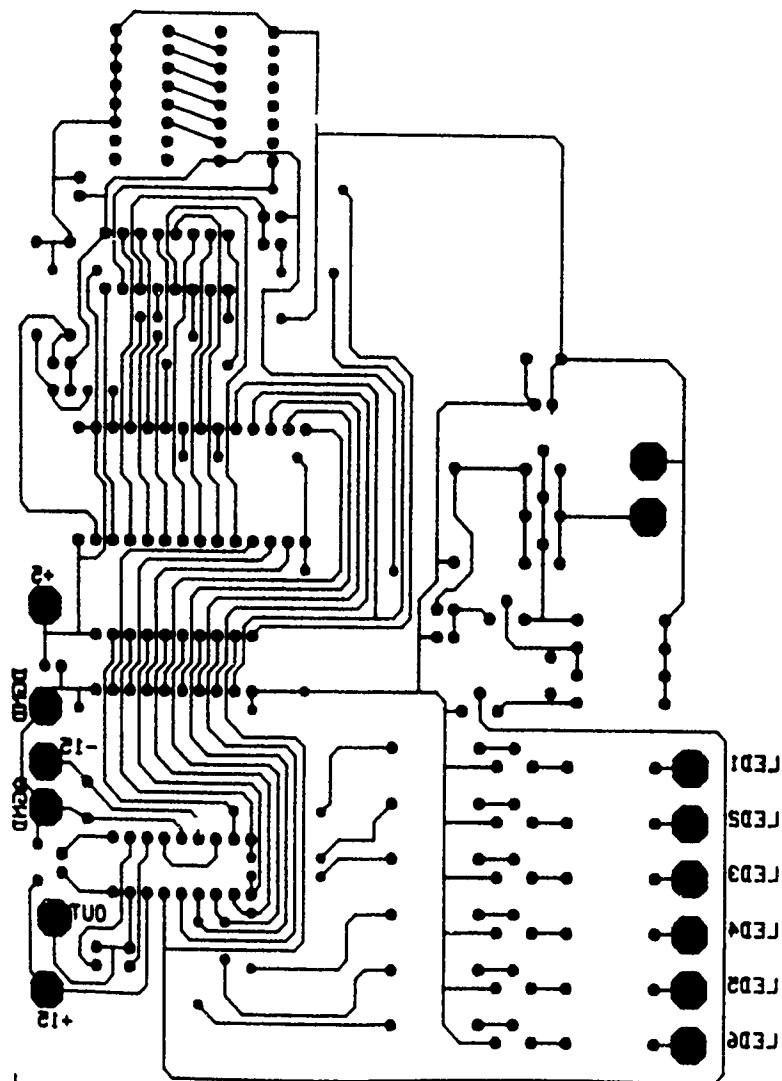
**Table 4: Receiver and 1PPR Receiver Cards Parts List**



TITLE <b>SIMULATOR BOARD COMPONENT LAYOUT</b>				FILENAME BLANK PLT
FILEDATE 07-Jul-1989				
FIGURE 24	FIGURE SHEET 1 of 1	DESIGNER JMA	DRAWN BY SPF	FILETIME 07 49 06
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Figure 24: Simulator Board Component Layout



TITLE <b>SIMULATOR BOARD ARTWORK</b>					FILENAME <b>BLANK.PLT</b>	UDRI University of Dayton Research Institute Electronic Computer Development Laboratory
FIGURE <b>25</b>	WEF 1 or 1	DESIGNER <b>JMA</b>	DRAWN BY <b>JK</b>	FILEDATE <b>01-Jul-1989</b>	PICTRM <b>07-19-06</b>	

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Figure 25: Simulator Board Artwork

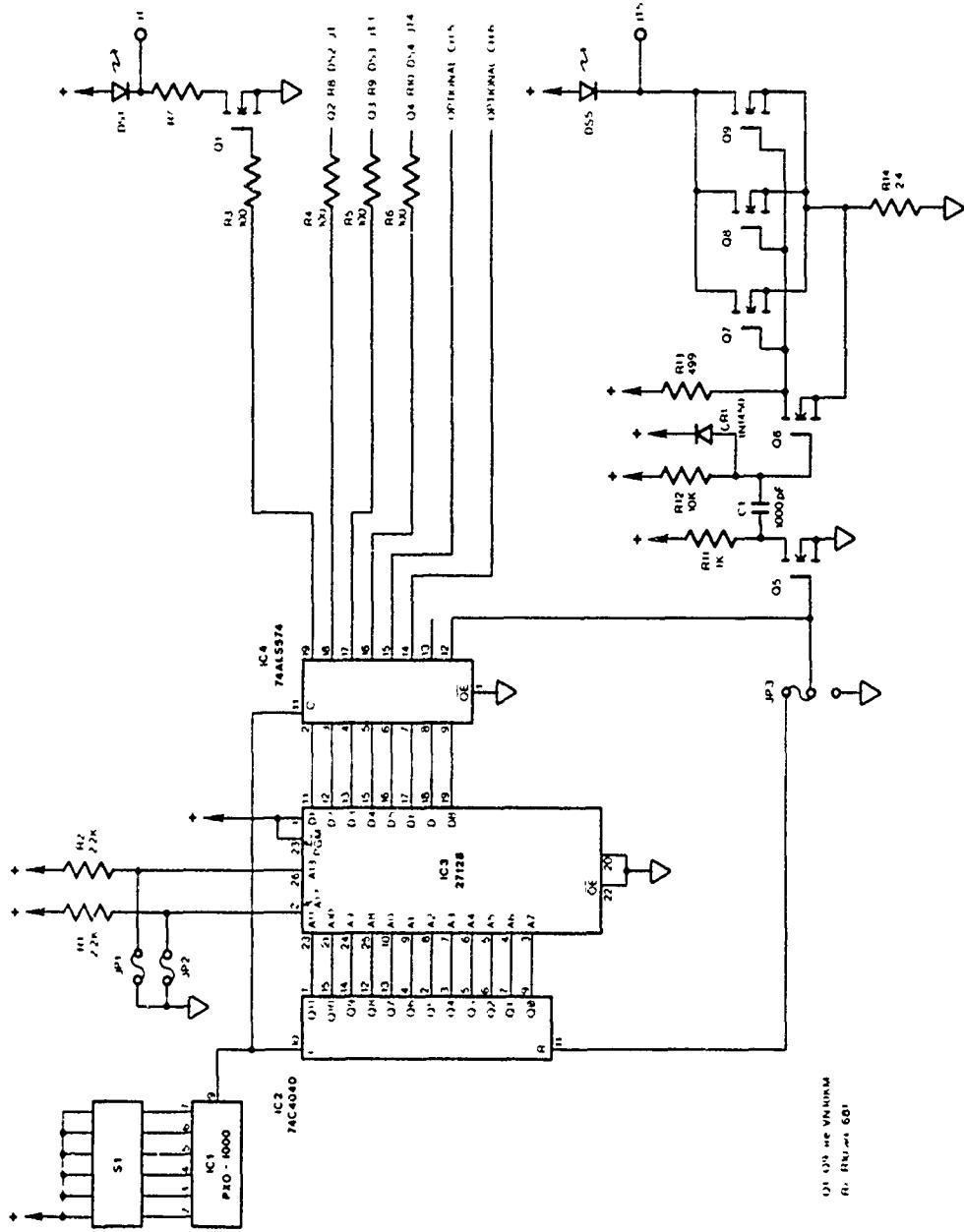


Figure 26: Simulator Board Schematic Diagram

FILENAME: BLANK PLT

FILEDATE: 07-JUL-1989

DESIGNER: JMA

DRAWN BY: SPF

FIGURE: 26

FILETIME: 07-49-06

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Figure 26: Simulator Board Schematic Diagram

Simulator Board Parts List

Part Number	Description
R1, R2	2.2 KOhm
R3 - R6	100 Ohm
R7 - R10	681 Ohm
R11	1 KOhm
R12	10 KOhm
R13	499 Ohm
R14	2.4 Ohm
C1	1000 pF
IC1	PXO-1000
IC2	74C4040
IC3	27128
IC4	74ALS574
Q1 - Q9	VN10KM
DS1 - DS5	LED
CR1	1N4150

Table 5: Simulator Board Parts List

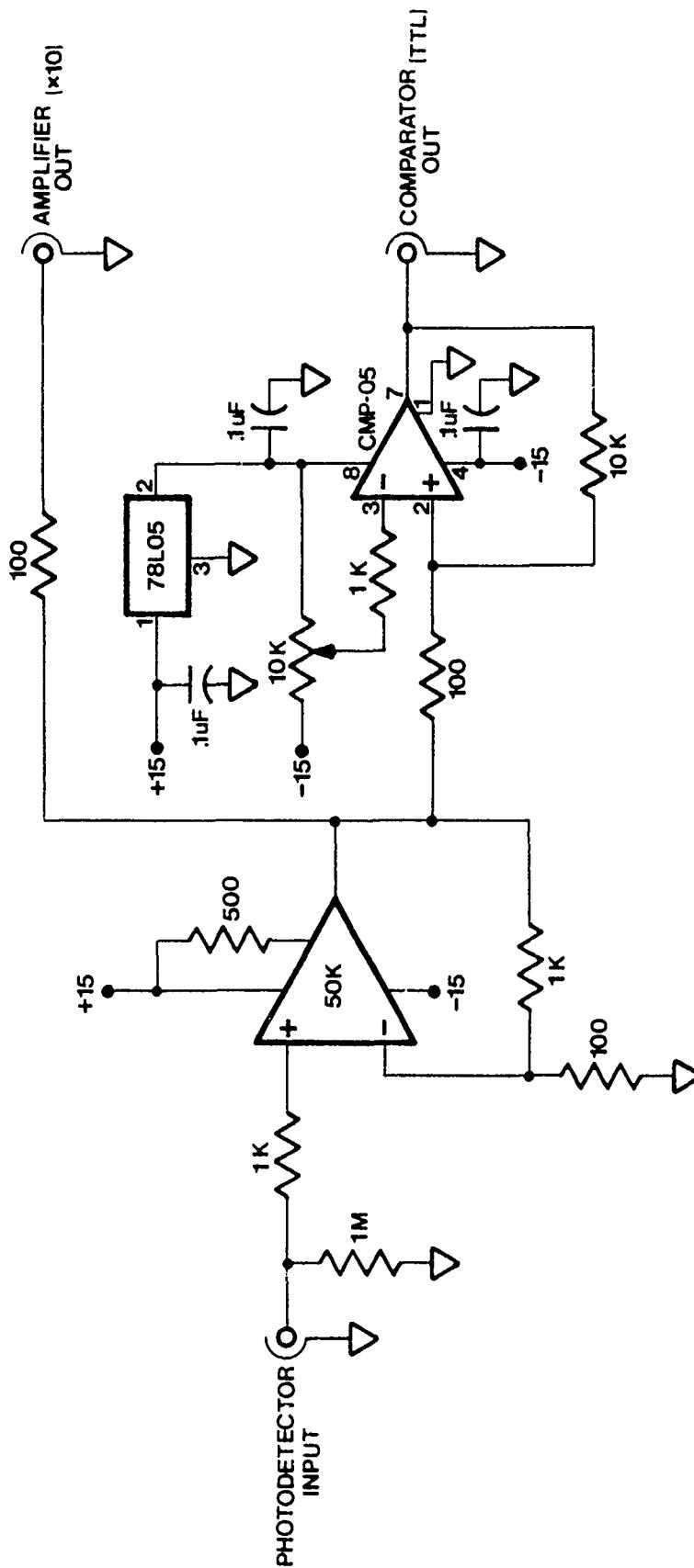


Figure 27: 1PPR Amplifier Schematic Diagram

## TURBINE BLADE BACKPLANE

FRONT		CLOCK	CHAN 1	CHAN 2	CHAN 3	CHAN 4
1	INPUT	PHOTODIODE	PMT 1	PMT 2	PMT 3	PMT 4
2	ANA2	ANA GND	ANA GND	ANA GND	ANA GND	ANA GND
3	ANA3					
4	ANA4					
5	ANA GND	ANA GND	ANA GND	ANA GND	ANA GND	ANA GND
6	+15V	+15V	+15V	+15V	+15V	+15V
7	-15V	-15V	-15V	-15V	-15V	-15V
8	COMP EN	COMP EN	COMP EN	COMP EN	COMP EN	COMP EN
9	LATCH EN	LATCH EN	LATCH EN	LATCH EN	LATCH EN	LATCH EN
10	ERROR RESET	E RESET	E RESET	E RESET	E RESET	E RESET
11	ERROR	ERROR	ERROR	ERROR	ERROR	ERROR
12	DIG GND	DIG GND	DIG GND	DIG GND	DIG GND	DIG GND
13	+5V	+5V	+5V	+5V	+5V	+5V
14	CNT LATCH	CNT LATCH	CNT LATCH	CNT LATCH	CNT LATCH	CNT LATCH
15	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK
16	CLOCK/	CLOCK/	CLOCK/	CLOCK/	CLOCK/	CLOCK/
17	C23	COUNTER BIT 23	C23	C23	C23	C23
18	C22	COUNTER BIT 22	C22	C22	C22	C22
19	C21	COUNTER BIT 21	C21	C21	C21	C21
20	C20	COUNTER BIT 20	C20	C20	C20	C20
21	C19	COUNTER BIT 19	C19	C19	C19	C19
22	C18	COUNTER BIT 18	C18	C18	C18	C18
23	C17	COUNTER BIT 17	C17	C17	C17	C17
24	C16	COUNTER BIT 16	C16	C16	C16	C16
25	C15	COUNTER BIT 15	C15	C15	C15	C15
26	C14	COUNTER BIT 14	C14	C14	C14	C14
27	C13	COUNTER BIT 13	C13	C13	C13	C13
28	C12	COUNTER BIT 12	C12	C12	C12	C12
29	C11	COUNTER BIT 11	C11	C11	C11	C11
30	C10	COUNTER BIT 10	C10	C10	C10	C10
31	C9	COUNTER BIT 9	C9	C9	C9	C9
32	C8	COUNTER BIT 8	C8	C8	C8	C8
33	C7	COUNTER BIT 7	C7	C7	C7	C7
34	C6	COUNTER BIT 6	C6	C6	C6	C6
35	C5	COUNTER BIT 5	C5	C5	C5	C5
36	C4	COUNTER BIT 4	C4	C4	C4	C4
37	C3	COUNTER BIT 3	C3	C3	C3	C3
38	C2	COUNTER BIT 2	C2	C2	C2	C2
39	C1	COUNTER BIT 1	C1	C1	C1	C1
40	C0	COUNTER BIT 0	C0	C0	C0	C0

Table 6: Detector/Electronics Chassis Backplane Pinout

**SIMULATOR CONNECTOR PINOUT**

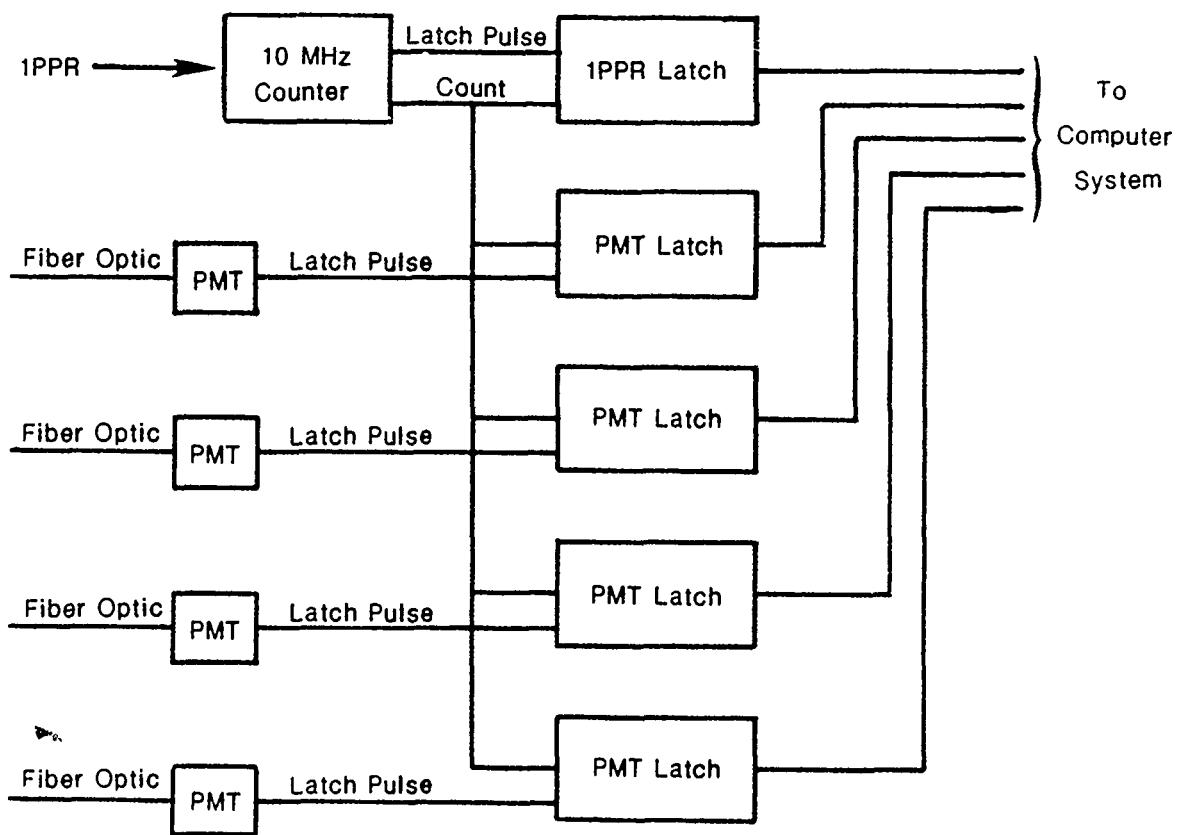
A	LED 1
B	LED 2
C	NC
D	LED 4
E	GND
F	1PPR LED
G	NC
H	GND
I	NC
J	GND
K	GND
L	NC
M	GND
N	LED 3

**Table 7: Simulator Connector Pinout**

RS-232 Connector Pinouts

1	Shield
2	Transmit
3	Receive
4	NC
5	NC
6	NC
7	Signal Ground
8	NC
9	NC
10	NC
11	NC
12	NC
13	NC
14	NC
15	NC
16	NC
17	NC
18	NC
19	NC
20	NC
21	NC
22	NC
23	NC
24	NC
25	NC

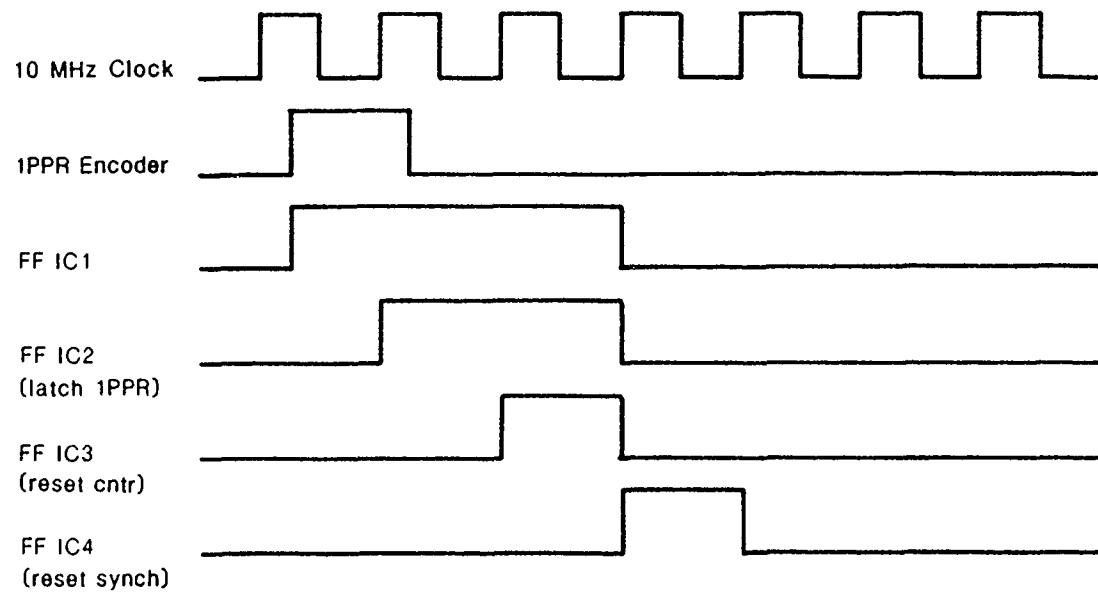
Table 8: RS-232 Connection Pinouts



TITLE DETECTOR/ELECTRONICS CHASSIS BLOCK DIAGRAM				FILENAME BLANK PLT
FIGURE 28				FILEDATE 07-Jul-1989
FIGURE 28	1 of 1	DESIGNER ECD	DRAWN BY MJG	FILETIME 07 49 06
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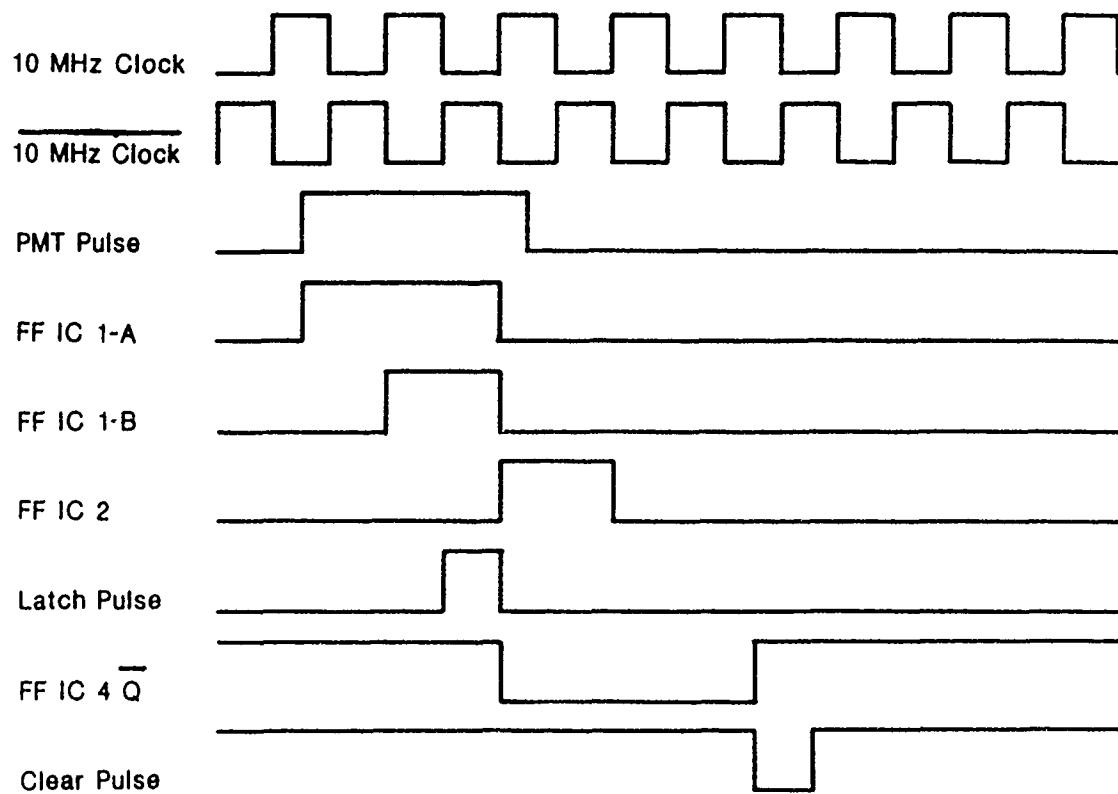
Figure 28: Detector/Electronics Chassis Block Diagram



TITLE <b>COUNTER SYNCHRONIZATION TIMING DIAGRAM</b>				FILENAME BLANK.PLT
FIGURE 29	FILEDATE 07-Jul-1989	DESIGNED MJD	DRAWN BY MJD	FILETIME 07 49 06
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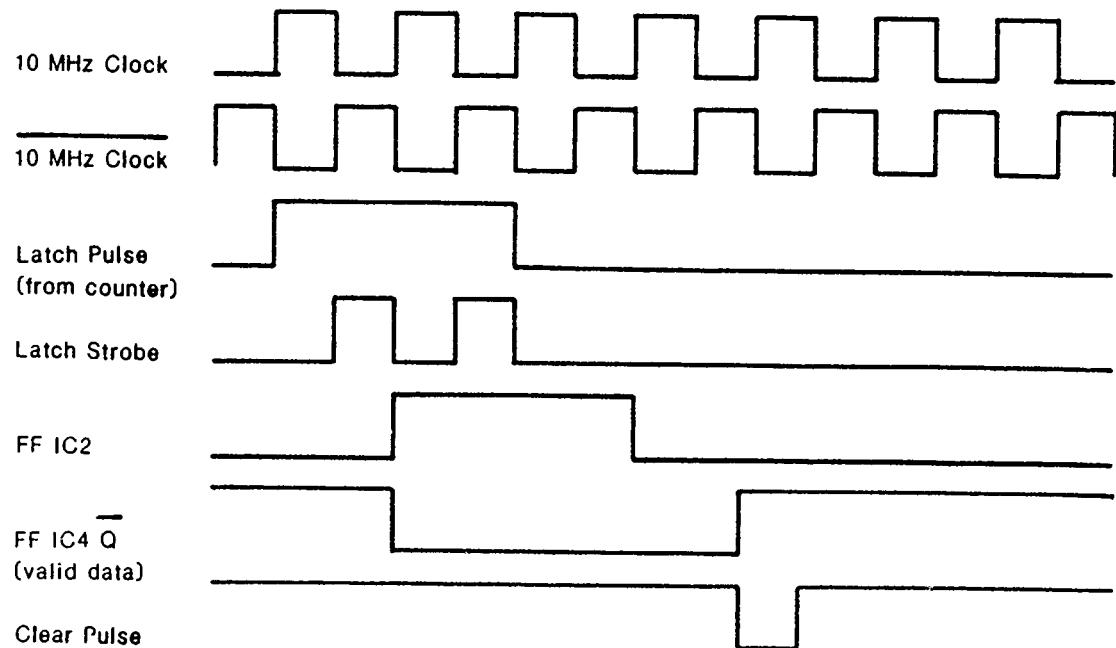
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Figure 29: Counter Synchronization Timing Diagram



TITLE LATCH CARD TIMING DIAGRAM				FILENAME BLANK PLT	FILEDATE 07-Jul-1989	FILETIME 07 49 06	UDRI University of Dayton Research Institute Electronic & Computer Development Laboratory
FIGURE 30	HEET 1 of 1	DESIGNER	DRAWN BY MJG				
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Figure 30: Latch Card Timing Diagram



TITLE <b>1PPR LATCH CARD TIMING DIAGRAM</b>				FILENAME <b>BLANK.PLT</b>
FIGURE <b>31</b>	SHEET 1 OF 1	DESIGNER	DRAWN BY <b>MJG</b>	FILEDATE <b>07-JUL-1989</b>
				FILETIME <b>07 49 06</b>
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Figure 31: 1PPR Latch Card Timing Diagram

NSMS Data Acquisition System - Tape Format

Fixed length - 512 byte records

block 0

```
bytes 0.. 3      : nb = number of blades
bytes 4.. 7      : nr = number of revolutions
bytes 8.. 11     : ns = number of stations
bytes 12.. 15    : average speed
bytes 16.. 19    : minimum speed
bytes 20.. 23    : maximum speed
bytes 24..127   : unused
bytes 128..136  : run date (DD-MMM-YY)
bytes 137..141  : excitation frequency
bytes 142..149  : run time (HH:MM:SS)
bytes 150..165  : radius
bytes 166..245  : run description
bytes 246..261  : run id
bytes 262..421  : specimen description
bytes 422..437  : specimen id
bytes 438..511  : unused
```

nbrd = number blocks for rev data = int((nr + 127)/128)

nbbd = number blocks for blade data = int((nr\*nb+127)/128)

block 1..nbrd

```
bytes 0..3      : rev 1 time for station 1
bytes 4..7      : rev 2 time for station 1
.
```

block nbrd+1..nbrd+nbbd

```
bytes 0..3      : rev 1 blade 1 time for station 1
bytes 4..7      : rev 1 blade 2 time for station 1
.
```

bytes nb\*4-4..nb\*4-1 : rev 1 blade nb time for station 1 bytes nb\*4..nb\*4+1 : rev 2 blade 1 time for station 1 .
.

repeat from block 1 for station 2, 3 and 4

tape mark

Table 9: Magnetic Tape Record Format